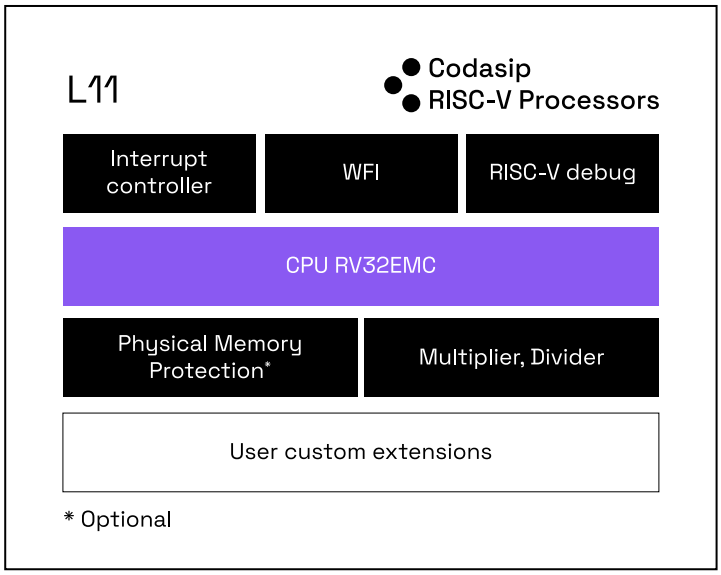
L11
Product brief

Codasip

Overview

The Codasip® L11 core is our smallest RISC-V core and an extremely efficient implementation of the Codasip Series 1.

It is ideal for low-power applications where silicon area matters in a broad range of devices.



The L11 core can be licensed either as an off-the-shelf (RTL and software toolchain) or fully customizable processor (CodAL).

Benefits

→ Entry-level RISC-V core

Ideal 32-bit, power efficient core for replacing existing 8- or 16-bit cores

→ Area player

Tiny 32-bit core ideal in simple, cost-sensitive devices

→ Designed for differentiation

RISC-V core designed in CodAL™, fully customizable with an architecture license

Applications

→ AI/ML

→ Wearables

→ Small IoT devices

Deliverables

- → Hardware Development Kit
- → Software Development Kit
- → FPGA evaluation platform
- → Basic set of applications
- → Documentation

Specifications

Core
3-stage, in-order pipeline, single issue
RV32E (CM) ISA
16-bit registers

Interrupts
Interrupt controller
Standard RISC-V CLINT implementation
Up to 128 interrupts
WFI
NMI

Debug
Standard RISC-V debug
2/4 JTAG pins
2-8 breakpoints & watchpoints
System bus access

Multiplier/Divider
Multiplier implementation: Sequential
Divider implementation: Sequential

Memory protection
Physical memory attributes with 2/4/8/16 regions
Machine privilege mode

Power
Clock gating
Configurable reset

Interface
AHB-Lite

Performance
Performance monitors

Customization

→ L11 is designed using Codasip Studio™

Easy customization in CodAL

→ Add new instructions or data types accelerating your algorithm

Studio automatically generates the compiler aware of such extensions

→ Connect your existing accelerator directly to the processor

Studio generates the RTL with the new interface