# Unlocking the potential of RISC-V with HW/SW co-design

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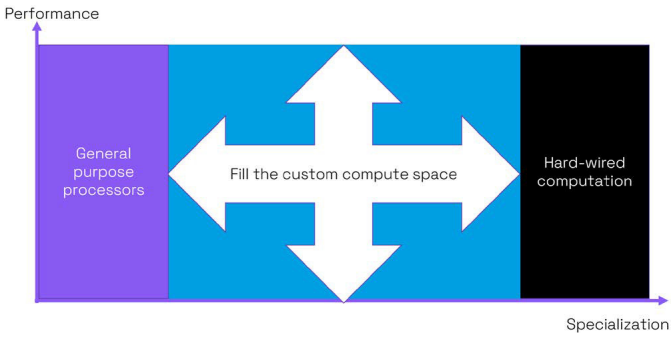
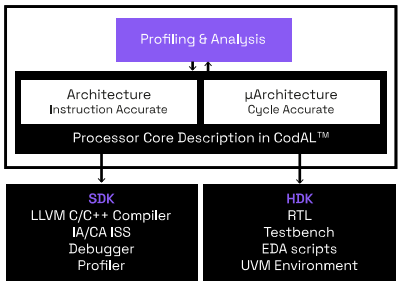
## → Custom compute with RISC-V is a huge opportunity space

Architectural innovation with custom instructions and tailored microarchitecture.



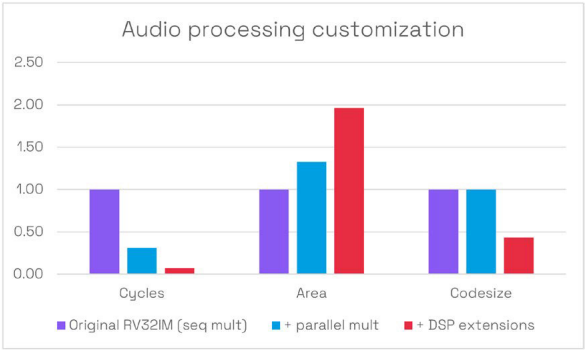

## → Automating HW/SW co-design

- Match hardware to software workload
- Take existing RISC-V description in CodAL
- Profile software to identify hotspots




- Refine instruction set regenerate SDK and profile
- Tailor microarchitecture to achieve goals and generate RTL & TB
- Verify custom RISC-V core

## → Audio processing example- design exploration and DSP custom instructions




- Customer looking to design new generation audio processing SoC
- Looking to replace Cortex-M
- Started with simple L30 configuration
- Used Studio to profile echo cancellation application
- Developed >40 custom DSP instructions
- Significant performance and code size improvement
- Relatively small area penalty

## → Convolutional neural network (CNN) example – custom instructions and accelerator HW

- IoT edge image recognition
- Limited resources with embedded core
- Profiled CNN using Studio
- Developed FIFO register chain for incoming pixel stream
- Custom instructions to accelerate convolution
- Significant performance and power improvement for acceptable area penalty