Effortless DSP extensions design for embedded RISC-V processors

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→ Codasip Studio and RISC-V Processors

Begin with a standard core
- Embedded and application cores
- High quality, production-ready
- Fully RISC-V compliant

Differentiate with Codasip Studio
- Configure / Customize
- Using CodAL architecture description language

→ DSP accelerators implemented with CodAL

- FIR filter accelerator
- Median filter accelerator
- FFT accelerator
- CORDIC accelerator

How DSP customization affects the PPA

Customizations with CodAL and Codasip studio shorten the time to market by providing out-of-the-box SDK and HDK tools and more compact core description. The table lists the code size and the human effort required to implement the described DSP customizations.

DSP-specific customizations of embedded RISC-V cores that tackle several representative DSP algorithms have improved the performance and energy consumption by 14.4x & 0.27x (FFT), 14.4x & 0.1x (FIR), 30x & 0.03 (Median filtering) and 24.3x & 0.08x (CORDIC), all at reasonable silicon area cost.

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