Codasip and Avery Partner to Improve Regression Test Methodology of RISC-V Processors

Brno, Czech Republic – November 8th 2017 – Codasip, the leading supplier of RISC-V® embedded CPU cores, today announced its partnership with Avery Design Systems, the provider of cutting-edge verification intellectual property (VIP) solutions for SoC and IP companies.

Codasip develops licensable RISC-V processors, the Berkelium (Bk) series, via a unique customization tool called Codasip Studio, allowing for fast configuration and optimization of the cores. Studio enables practically an endless number of RISC-V variants, which places extensive demands on verification.

"With the flexibility of Codasip Studio, extensive verification becomes essential, and we are constantly on the lookout for innovative VIP solutions that will make a part of the verification process faster, easier, or more reliable," says Marcela Zachariášová, the VP of Verification at Codasip. "Avery Design Systems offer some very useful features."

Specifically, Codasip employs the Avery VIP fault injection feature**,** which introduces random or precisely-planned faults into the communication lines between the processor and the surrounding components. This allows simulation of unexpected corner cases. Such stress testing is vital to ensure that the processors are robust and reliable even when faults occur.

"We need to ensure that all variants of our RISC-V processors handle error scenarios correctly and can respond to any type of error from the surrounding components without crashing or freezing. Avery's fault injection helps us analyze such scenarios in our cores," explains Mrs. Zachariášová.

Codasip itself, and with assistance of industry alliances, has introduced innovations in the field of verification, achieving best-in-class results in verification automation and acceleration. The recent introduction of Avery's fault injection technology has helped to further improve Codasip's regression methodology.

"We have partnered with Avery because of unique benefits their fault injection technology brings," concludes Mrs. Zachariášová.

About Codasip

Codasip delivers leading-edge processor IP and high-level design tools that provide ASIC designers with all the advantages of an open standard, such as the RISC-V ISA, along with the unique ability to automatically optimize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and GNU based processor solutions, Codasip is committed to open standards for embedded processors.

Formed in 2006 and headquartered in Brno, Czech Republic, Codasip currently has offices in the US and Europe, with representatives in Asia and Israel.

For more information about Codasip's products and services, visit www.codasip.com.

About Avery

Founded in 1999, Avery Design Systems, Inc. enables system and SoC design teams to achieve dramatic functional verification productivity improvements through formal analysis applications for RTL and gate-level X verification, and robust verification IPs for PCI Express, USB, AMBA, UFS, MIPI, DDR/LPDDR, HBM, HMC, ONFI/Toggle, NVM Express, SCSI Express, SATA Express, eMMC, SD/SDIO, Unipro, CSI/DSI, Soundwire, and CAN FD standards.

Avery is headquartered in Tewksbury, Massachusetts, and operates an R&D center in Taipei, Taiwan. Avery's products are directly marketed and distributed in the US, Europe, Japan, Korea, and Taiwan.

For further information about Avery Design Systems, visit www.avery-design.com.