Codasip Announces Studio 7, Design and Productivity Tools for Rapid Generation of RISC-V Processors

Brno, Czech Republic – January 23rd, 2018 – Codasip, the leading supplier of RISC-V® embedded processor IP, today announced that it has launched the 7th generation of its Studio, the unique IP-design and customization software that allows for fast configuration and optimization of RISC-V processors, customer-proprietary processor architectures, and their accompanying software development toolchains.

Studio 7 adds significant new functionality and features, making it the most advanced and effective technology on the market for tailoring RISC-V processors to meet chip designers' application-specific needs. Codasip engineers have used the Studio design flow to create the broadest portfolio of RISC-V processors in the industry, and they now put the power in the hands of customers to further customize and extend the RISC-V instruction set, based on the unique requirements of the algorithms being run.

Studio can be used for

- processor prototyping for a specific application domain,
- fast design space exploration,
- development of custom extensions using Codasip's architecture description CodAL language.

Studio then generates hardware and corresponding SDKs that are aware of the custom extensions, including

- Verilog or VHDL RTL and System Verilog UVM environments,
- testbenches and synthesis scripts,
- full compiler toolchain including advanced profiling and debugging tools,
- both cycle-accurate and fast instruction-accurate simulation tools.

Some of the new features included with Studio 7:

- Native support for industry-standard AMBA interfaces, allowing for easy replacement of other processor cores while reusing your existing, proven peripheral IP.
- IEEE 1149-7-compatible 2-wire JTAG to minimize pin-count.
- Improvements in clock-gating for low-power requirements.
- Major updates to Codespace, the optional Eclipse-based IDE, and the underlying software tools, including support for LLVM 5.0.

"Studio 7 is a big step forward for Codasip's advanced processor creation technology, and will take the guesswork out of implementing the ever-expanding number of ISA options in the RISC-V specification. Studio can help generate processors well-suited to the widest range of application areas, from machine learning inference engines to host processor DSP offload, networking, and storage," stated Karel Masařík, CEO and co-founder of Codasip. *"With Studio 7, there is no need to settle for a one-size-fits-all processor."*

The ***Studio 7*** processor design and customization tool suite is available now.

About RISC-V

RISC-V is an open, free instruction set architecture (ISA) enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

For more information about RISC-V, visit www.riscv.org.

About Codasip

Codasip delivers leading-edge processor IP and high-level design tools that provide ASIC designers with all the advantages of the RISC-V open-standard ISA, along with the unique ability to automatically optimize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded processors.

Formed in 2006 and headquartered in Brno, Czech Republic, Codasip currently has offices in the US and Europe, with representatives in Asia and Israel.

For more information about Codasip's products and services, visit www.codasip.com.