Codasip Releases Studio 8, a Breakthrough in RISC-V Automation, and the Bk7 RISC-V Processor Core for Real-Time Computing Applications

Munich, Germany – December 6th, 2018 – Codasip GmbH, the leading supplier of RISC-V® embedded processor IP, announced today the latest version of Studio, a suite of tools optimized for the development and verification of RISC-V processors, and the Bk7 processor, the first Codasip RISC-V core optimized for Linux and real-time performance.

"As the RISC-V ISA specification evolves and adds an ever-increasing number of optional architecture extensions, a processor design methodology that allows for both rapid architectural exploration and simplified creation of easily implementable RTL becomes essential," stated Chris Jones, Vice President of Marketing at Codasip. "*What is needed is a high-level processor description language optimized for RISC-V, so Codasip has delivered Studio 8, a comprehensive tools suite for RISC-V processor development."*

With Studio, designers write a high-level description of a processor in CodAL, an architecture description language, and then automatically synthesize the design's RTL, test bench, virtual platform models, and processor SDK (C/C++ compiler, debugger, profiler, etc.). Time that would otherwise be required to maintain a complete SDK and implementation is significantly reduced thanks to the methodology that uses an Instruction Accurate (IA) processor model in CodAL for SDK generation and a Cycle Accurate model for implementation.

Codasip employs this silicon-proven methodology to create and deliver a broad portfolio of licensable RISC-V processor IP. Through these product developments, Studio has evolved to make it more suitable for implementing and extending the instruction set of RISC-V cores. The 8th generation of Codasip Studio, just announced, adds significant new functionality and features, making it the most advanced and effective technology on the market for tailoring RISC-V processors to meet chip designers' application-specific needs. Specifically, Studio 8 includes:

- Support for LLVM debugger (LLDB) and OpenOCD,
- LLVM 7.0,
- Studio/CodeSpace IDEs based on Eclipse Oxygen along with more interactive consoles,
- improved test suites and verification to better support user-defined RISC-V extensions.

Further, Codasip architects employed Studio to develop the Bk7 processor, the latest RISC-V micro-architecture in the Codasip portfolio.

A 64-bit machine featuring a balanced 7-stage pipeline with branch prediction, optional full MMU with virtual addressing support for operating systems such as Linux, and support for the popular RISC-V standard extensions as well as industry-standard external interfaces, the Bk7 is Codasip's highest-performance processor to date and is ideal for system-on-chip designers who need the right balance of power and performance. Also, the Bk7 is fully customizable so architects can easily add additional instructions, registers or interfaces. And as with each member of the Codasip Bk processor family, the Bk7 comes with the following deliverables:

- Readable Verilog or VHDL RTL along with test benches and synthesis scripts,
- SDK consisting of LLVM-based compiler, advanced profiling and debugging tools,
- both cycle-accurate and fast instruction-accurate simulation tools.

Studio 8 and the Bk7 processor are generally available in the first quarter of 2019, with early access to selected customers immediately.

About Codasip

Codasip delivers leading-edge processor IP and high-level design tools that provide ASIC designers with all the advantages of the RISC-V open-standard ISA, along with the unique ability to automatically optimize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded processors.

Formed in 2006 with research and development located in Brno, Czech Republic, Codasip currently has offices in the US and Europe, with representatives in Asia and Israel. Codasip is currently venture-backed by Credo Ventures, Ventech Capital, Shenzhen Capital, Paua Ventures, and Western Digital.

For more information about Codasip's products and services, visit www.codasip.com.

About RISC-V

RISC-V is an open, free instruction set architecture (ISA) enabling a new era of processor innovation through open-standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

For more information, visit www.riscv.org.