CODASIP TO DEMONSTRATE TECHNOLOGY LEADERSHIP AND COMMITMENT TO OPEN STANDARDS AT TAIWAN RISC-V WORKSHOP

Munich, Germany – March 7, 2019 – Codasip GmbH, the leading supplier of configurable RISC-V® embedded processor IP, will address the topics of RISC-V C compiler optimizations and frameworks for ISA compliance in two presentations at the upcoming RISC-V Workshop in Taiwan.

In the first presentation, Codasip CTO Zdeněk Přikryl will demonstrate how Codasip generates and optimizes the latest LLVM version 7.0.1 toolchain to make use of custom instructions, including debugging and profiling. The LLVM project continues to expand rapidly as industry leaders have chosen to adopt LLVM compiler due to its excellent quality of results. While many employ various components of the LLVM toolchain, Codasip has announced availability of LLVM for compilation, code generation, and debugging for its family of RISC-V processors. Full support for LLDB in command-line mode or as part of an Eclipse-based graphical debug is now part of its latest generation of licensable software development tools.

In the second presentation, Codasip engineer Milan Skála will discuss requirements for a RISC-V compliance test framework that could be employed for any valid implementation of the RISC-V standard. He will show Codasip's methodology as an example. Based on Python's pytest, it provides golden reference model configuration, including test suite builds along with test suite parametrization, compilation, run control with results evaluation, and compliance test reports.

Karel Masařík, Codasip's founder and CEO, said: *"By addressing the topics of compiler optimizations and ISA compliance testing, Codasip is emphasizing its commitment to open standards for embedded processors. We are dedicated to making meaningful contributions to the RISC-V community to ensure that the ecosystem grows and benefits the entire industry. At the same time, we will of course continue to innovate with our own Codasip Studio which allows for rapid development of optimized and differentiated processor IP."*

The RISC-V Workshop Taiwan takes place on 12–13th March 2019 in the Ambassador Hotel, Hsinchu City, Taiwan. More information about registration and agenda can be found at the event webpage: https://tmt.knect365.com/risc-v-workshop-taiwan/

Codasip GmbH
Paul-Gerhardt-Allee 50
81245 Munich, Germany

Codasip R&D Center
Božetěchova 1/2, 612 00 Brno
Czech Republic

Phone: +420 541 141 475
E-mail: contact@codasip.com
Website: www.codasip.com

About Codasip

Codasip delivers leading-edge processor IP and high-level design tools, providing ASIC designers with all the advantages of the RISC-V open ISA, along with the unique ability to automatically optimize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and

GNU-based processor solutions, Codasip is committed to open standards for embedded processors. Formed in 2006 and headquartered in Brno, Czech Republic, Codasip currently has offices in the US and Europe, with representatives in Asia and Israel. For more information about Codasip's products and services, visit www.codasip.com.

About RISC-V

RISC-V (pronounced "risk-five") is an open, free ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation. For more information about RISC-V, visit www.riscv.org.

Media Contact

Chris Jones, VP of Marketing
E-mail: jones@codasip.com