CODASIP PRESENCE AT UPCOMING EVENTS: CHINA ROADSHOW, DAC 2019, AND RISC-V WORKSHOP ZURICH

Munich, Germany – May 6th, 2019 – Codasip GmbH, the leading supplier of configurable RISC-V® embedded processor IP, is going to be featured at three major industry events around the globe in the second quarter of 2019: China Roadshow 2019, Design Automation Conference in Las Vegas, and RISC-V Workshop in Zurich.

"Getting Started with RISC-V" Roadshow 2019, May 6–16, is a series of events taking place in five cities across China in eleven days. The show aims to present entry-level examples of innovative RISC-V solutions, and attendance is free of charge. Codasip is co-sponsoring the event and will have **Tina Xiang, China General Manager**, speaking about Codasip's smart solutions and tools for automated generation and customization of RISC-V processors. Tina's presentation starts at 10:00 each day of the main show schedule:

- Wednesday, **May 8**, Sheraton Chengdu Lido Hotel
- Monday, **May 13**, Hyatt on the Bund, Shanghai
- Tuesday, **May 14**, JW Marriott Hotel Hangzhou
- Thursday, **May 16**, Crowne Plaza Zhongguancun Beijing

For more information about the event, visit https://www.lfasiallc.com/events/risc-v-china-roadshow-2019/.

Design Automation Conference 2019, June 2–6 at the Las Vegas Convention Centre in Las Vegas, Nevada, is the premier conference devoted to the design and automation of electronic systems (EDA), embedded systems and software (ESS), and intellectual property (IP). The event will offer close to 300 technical presentations, training sessions, workshops, and an exhibition area featuring of around 200 companies. Codasip's **VP of Worldwide Sales, Jerry Ardizzone**, will be presenting his views on the future commercial success of open ISAs as a guest of a panel discussion on Tuesday, **June 04**, at **10:30**. Detailed info on the discussion topic available at http://www2.dac.com/events/eventdetails.aspx?id=267-19.

RISC-V Workshop Zurich, June 11–13 at ETH Zurich (Swiss Federal Institute of Technology), is organized by the RISC-V Foundation and again co-sponsored by Codasip. The presentation will be given by **Zdeněk Přikryl, Codasip CTO**, who will explain the benefits of the open source compiler technologies developed within the LLVM project, and how Codasip integrates the LLDB debugger in its automated toolchain. His presentation is scheduled for Wednesday, **June 12,** at **17:40**. More information about the presentation can be found at https://tmt.knect365.com/risc-v-workshop-zurich/agenda/2#commercial-offerings_configurable-lldb-debuggers-for-risc-v.

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About Codasip

Codasip delivers leading-edge processor IP and high-level design tools, providing ASIC designers with all the advantages of the RISC-V open ISA, along with the unique ability to automatically optimize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and

GNU-based processor solutions, Codasip is committed to open standards for embedded processors. Formed in 2006 and headquartered in Brno, Czech Republic, Codasip currently has offices in the US and Europe, with representatives in Asia and Israel. For more information about Codasip's products and services, visit www.codasip.com.

About RISC-V

RISC-V (pronounced "risk-five") is an open, free ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation. For more information about RISC-V, visit www.riscv.org.

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