QUESTA SLEC TOOL FROM MENTOR, A SIEMENS BUSINESS, TO HELP CODASIP SPEED UP VERIFICATION OF MULTIPLE HDL OUTPUTS

Codasip GmbH, the leading supplier of configurable RISC-V® embedded processor IP, has selected Questa® SLEC by Mentor for use as part of its comprehensive verification flow. The Codasip verification team expects this will significantly reduce the time needed to ensure logical equivalence of multiple HDL representations of each of its processors.

What is Questa SLEC

Questa SLEC was designed to perform a fast and reliable sequential logic equivalence check (SLEC). The purpose of SLEC is to verify that two designs that differ sequentially but are supposed to be functionally equivalent, really are equivalent — that is, they produce the same output for the same input in all cases. The Questa SLEC app performs SLEC by finding corresponding blocks of RTL code and comparing them through deep formal analysis. This formal-based approach outperforms even the best-designed simulation in speed and exhaustiveness, covering all scenarios including rare corner cases. This is a handy feature in many testing scenarios.

Design Process at Codasip

At Codasip, we design a new processor by first describing it in CodAL, our proprietary C-based language for processor architecture description. CodAL can then produce any common HDL code, including VHDL, Verilog, and SystemVerilog. All these must be thoroughly verified to ensure that they are functionally identical and correct. Questa SLEC will dramatically reduce the time required to guarantee that each representation is the same.

How the Questa SLEC App Can Help

The verification team at Codasip decided to use the Questa SLEC app to speed this process up. One of the HDL outputs, for example the Verilog code, will be thoroughly verified using UVM as before. All other HDLs, for example VHDL and SystemVerilog, will be verified using Questa SLEC to compare the code against the already verified one.

Benefits of the New Approach

As the formal analysis performed by Questa SLEC is very fast, the new approach should accelerate verification of any additional HDL from tens of hours to tens of minutes. In the case of three HDL outputs, whole days and considerable effort can be saved, bringing financial benefits as well as a competitive advantage to Codasip.

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