



# CODASIP AWARDED EUROPEAN UNION HORIZON 2020 FUNDING FOR DEVELOPING NEW RISC-V PROCESSORS

**Munich, Germany - 17th March 2020** – Codasip GmbH, the leading supplier of configurable RISC-V® embedded processor IP, announced today that it has received a Horizon 2020 award from the European Union. The award entitled RISC-V Digital Architecture for the Next Generation of Connected Era is aimed at developing processor cores for the rapidly growing market for integrated circuits for Internet of Things (IoT), connected cars, drones, and artificial intelligence.

European Union Horizon 2020 is the biggest Research and Development programme to date aimed at improving the competitiveness and leadership of the European industry & science. Codasip's award aims at strengthening the European position in low-power microcontrollers, Internet of Things, and computation for emerging smart applications. The award will enable Codasip to accelerate extending its processor product line from lower to medium-complexity embedded applications and more complex ones involving multicore and high-performance computing.

*"We are honored to have been chosen for the Horizon 2020 award and recognized as providing a strategic technology in Europe,"* stated Karel Masařík, CEO Codasip GmbH. *"We look forward to accelerating the development of the most advanced RISC-V cores."*

Codasip is a leading supplier of configurable RISC-V® embedded processor IP. Codasip provides a portfolio of various RISC-V implementations along with a suite of processor-developing tools to allow for rapid core customization. The company will also contribute to working groups on verification platforms and open cores. Codasip has based its processor development on describing instruction sets and microarchitecture in its high-level CodAL language and Codasip Studio product. Studio enables the automatic generation of RTL, software development tools, simulation models, and UVM descriptions from a CodAL description of the core.

RISC-V is an open, modular, extensible instruction set architecture (ISA) that can be applied to a wide range of applications, from simple embedded applications such as tags to high-performance computing. Codasip was a founding member of the RISC-V Foundation and launched its first RISC-V processor core in 2015.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 881172.



## About Cudasip

Cudasip delivers leading-edge processor IP and high-level processor design tools, providing ASIC designers with all the advantages of the RISC-V open ISA, along with the unique ability to automatically customize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and GNU-based processor solutions, Cudasip is committed to open standards for embedded processors. Formed in 2006 and headquartered in Munich, Germany, Cudasip currently has offices in the Europe, US, China and with representatives in Asia and Israel. For more information about our products and services, visit [www.codasip.com](http://www.codasip.com).

## About RISC-V

RISC-V (pronounced "risk-five") is an open, free ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation. For more information about RISC-V, visit [www.riscv.org](http://www.riscv.org).

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