Press Release

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CODASIP RELEASES THE FIRST LINUX-CAPABLE RISC-V CORE BK7 OPTIMIZED FOR DOMAIN-SPECIFIC APPLICATIONS

Munich, Germany – July 21st – Codasip, the leading supplier of customizable RISC-V® embedded processor IP, today announced the official release of Bk7, the most advanced core in the Codasip family of RISC-V processor IP to date, built specifically with customization and domain-specific optimization in mind. The Bk7 is ideally suited for any sophisticated modern application, from security to real-time AI processing, especially where embedded Linux is required.

The Codasip Bk7 is a 64-bit processor core with a single in-order 7-stage pipeline, fully compliant with the RV64IMAFDC instruction set architecture (ISA). As with all Codasip Bk cores, the open RISC-V standard makes it possible to configure and extend the core to precisely fit the customer's domain-specific needs.

"General-purpose processor architectures are not a good fit for many application areas and manufacturers are beginning to see that customized, domain-specific architectures beat them in almost every aspect," notes **Karel Masařík, CEO of Codasip**. *"So, our main aim with Bk7 was to make it the fastest and most customization-friendly design yet."*

RISC-V-based processors are customizable by design, but the customizability presents a challenge for chip manufacturers in terms of time-to-market. Any custom changes need to be reflected in the RTL code, the instruction set simulator and the compiler, and most importantly, the customized design must be thoroughly verified, which traditionally requires considerable time and effort.

Notably, the unique Codasip Studio toolset, used to design the Bk7, already makes the whole process faster and easier by automatizing all the mentioned tasks. Studio uses a single high-level description of a core written in CodAL, an easy-to-learn C-like language. Once this description is updated with any required custom changes, Studio will use it to automatically generate a complete customized HDK and SDK, including a full UVM verification environment—everything needed to deploy the core. With Bk7, Codasip has taken this unique approach a step further by developing a new, module-based architecture for even easier CodAL editing.

"For Bk7, we enhanced the CodAL language so that it can handle modularized design better, and we based the Bk7 architecture on modules," explains **Zdeněk Přikryl, Codasip CTO**. *"The modules are basically self-contained building blocks that represent various useful configuration options and can be readily added, removed, or reused across multiple designs. This means that customizing the CodAL description, which is the only non-automated step in Codasip Studio, becomes even simpler and faster. Codasip customers are now able to get a customized core with the best PPA for their domain in a hassle-free way that is truly innovative and unmatched in the industry."*

The off-the-shelf configuration of Bk7 includes support for the RISC-V atomic and floating-point extensions (both single and double precision), a memory management unit (MMU), and support for privilege modes needed for richer operating systems including Linux. Bk7 also features an internal interrupt controller, dynamic branch prediction (BHT, BTB, RAS), JTAG and RISC-V debug, and standard bus interfaces (AMBA). In-built customizable options include the branch predictor, instruction and data caches, store buffer, and others. Future releases of Bk7 will additionally include tightly coupled memories, dual issue microarchitecture, and multicore support.

The Bk7 comes in a package that contains all supporting tools to deploy the core: the CodAL description (fully editable in Codasip Studio), RTL code of the default configuration, the CodeSpace IDE to write software for the core, C compiler (LLVM and GCC), source files and compilation guide for Linux, and Linux boot demo SoC.

Bk7 is available for licensing now through the Codasip sales teams worldwide. For expert consultation and a quote, use the contact form at www.codasip.com/contact or get in touch directly via info@codasip.com.

About Codasip

Codasip delivers leading-edge processor IP and high-level processor design tools, providing ASIC designers with all the advantages of the RISC-V open ISA, along with the unique ability to automatically optimize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded processors. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has offices in Europe and China, with sales representatives worldwide. For more information about our products and services, visit www.codasip.com.

About RISC-V

RISC-V (pronounced "risk-five") is an open, free ISA enabling a new era of processor innovation through open standard collaboration. RISC-V enables you to take advantage of a standard base instruction set for software portability, yet a choice of standard or custom extensions to enhance computational performance. For more information about RISC-V, visit www.riscv.org.

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