Press Release

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Munich, Germany | Ottawa, Canada

CODASIP AND METRICS DESIGN AUTOMATION ANNOUNCE THE INTEGRATION OF THE METRICS CLOUD SIMULATION PLATFORM IN CODASIP'S RISC-V SWERV CORE™ SUPPORT PACKAGE PRO

Munich, Germany and Ottawa, Canada – August 5th 2020 – Codasip, the leading supplier of customizable RISC-V embedded processor IP, and Metrics Design Automation, providers of the only True Cloud EDA solution, today jointly announced the integration of the Metrics SystemVerilog RTL Simulation Platform within Codasip's Pro SweRV Core™ Support Package. This integration provides a very easy-to-use and inexpensive way for ASIC designers to verify modifications and enhancements they make to the SweRV embedded processor IP.

One of the major benefits of the open source RISC-V ISA is that it allows users to customize their processor IP for optimal implementation in domain-specific applications. With this valuable benefit however comes the responsibility to verify any changes made to the processor IP for functional accuracy. Codasip and Metrics have teamed together to address this requirement by making RTL verification available in the Cloud directly from the Codasip SweRV Core Support Package. SweRV and the Support Package users thus do not have to install and license any EDA software, do not have to make any expensive purchases of RTL simulation software, and have all the SweRV and verification IP required all preloaded in a Cloud cluster for immediate use.

"Codasip continues to expand its ecosystem for RISC-V embedded processor IP for the benefit of our customers," says **Karel Masařík, CEO of Codasip**. *"This integration of the Metrics Cloud Simulator in our SweRV Core Support Package is an example of making RTL verification easier and more affordable for Codasip customers and SweRV users."*

The Metric Cloud Simulator is a fully compliant SystemVerilog simulator and is the only RTL simulator available with a SaaS business model—users simply pay for use as a service. The implementation of Metrics simulator in the Cloud provides massive scalability so regression tests can run in parallel to complete in hours, not days.

"The popularity of RISC-V and in particular the SweRV open source processor IP has been impressive," noted **Doug Letcher, CEO of Metrics**. *"We are excited to partner with a leading RISC-V embedded processor IP vendor such as Codasip to deliver better usability, accelerated verification, and much more affordability of RTL simulation tools to the ASIC and SoC design community."*

The SweRV Core Support Package with Metrics Cloud Simulation integration is available now. For further information, use the contact form at www.codasip.com/contact or get in touch directly via info@codasip.com.

About Codasip

Codasip delivers leading-edge processor IP and high-level processor design tools, providing ASIC designers with all the advantages of the RISC-V open ISA, along with the unique ability to automatically optimize the processor IP. As founding member of the RISC-V Foundation and a long-time supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded processors. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has offices in Europe and China, with sales representatives worldwide. For more information about our products and services, please visit www.codasip.com.

About Metrics Design Automation

Metrics is the first true cloud-based platform for ASIC and complex FPGA design verification, uniquely providing massively scalable computing, elastic storage, and a SaaS business model. Established in 2017, Metrics is headquartered in Ottawa, Canada, and has offices throughout the United States and sales representatives worldwide. For more information, visit www.metrics.ca.

Media Contacts

Roddy Urquhart, Senior Marketing Director, Codasip
Email: rurquhart@codasip.com

Dan Ganousis, VP of Sales and Marketing, Metrics Design Automation
Email: dan.ganousis@metrics.ca