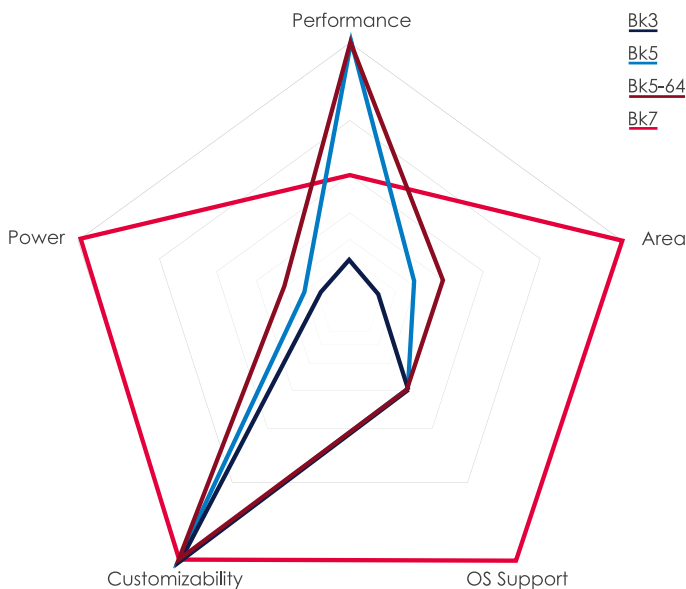


CODASIP RISC-V Processors

If you are looking for an off-the-shelf RISC-V core, we offer a range of microarchitectural implementations of the RISC-V standard for virtually any application requirements. Codalisp's own line of RISC-V processors, the **Bk family**, is fully verified and ready for instant deployment, or to be used as a quick-start base for customization with Studio.

BK CORES AT A GLANCE



RISC-V

The cornerstone of our processor family is the **RISC-V** ISA (instruction set architecture). It is an open, independent, royalty-free architecture that protects your investment in system software, thus minimizing risk.

Longevity

Established and supported by big industry players, RISC-V provides a strong, reliable, and growing ecosystem that is not dependent on a single vendor, which means that you will not have to face any incompatibilities and related redesign costs in the future. Traditional closed architectures now have a proven, credible alternative.

Innovation

Apart from being cost-efficient, RISC-V is also flexible. It includes base instructions that are always present, and a variety of standard extensions that you can choose from based on your specific needs. On top of that, RISC-V allows you to create novel custom instructions to achieve your performance, power or area goals and make your design truly unique.

THE ECOSYSTEM

Outstanding Software Infrastructure

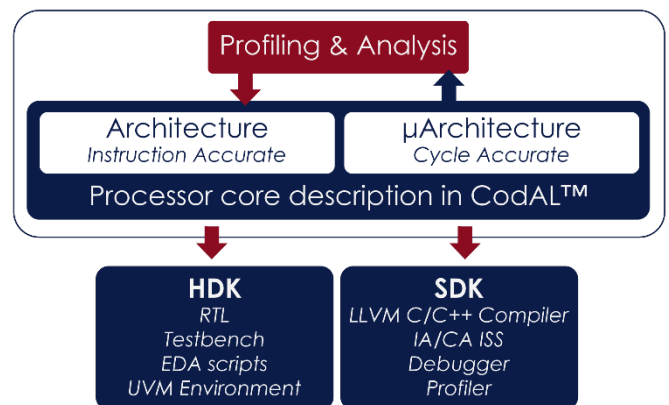
All Codalisp cores are supplied with an industry-leading development environment, **Codalisp CodeSpace**, for developing software to run on the designed processor. The IDE is based on the open Eclipse framework and it outperforms community alternatives across a wide range of benchmarks as we have added proprietary optimizations to its LLVM back-end.

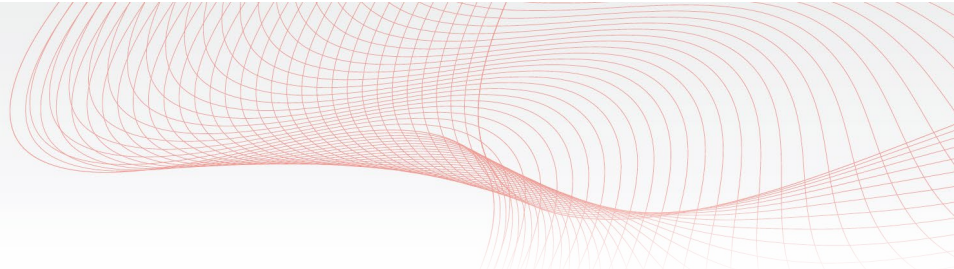
Codalisp CodeSpace includes a code editor, compiler, profiler, and debugger. You will get a 1-year license for free with any of our off-the-shelf RISC-V cores.

Customization with Studio

All Codalisp Bk processors are fully verified and ready for instant deployment, or to be used as a quick-start base for customization with **Codalisp Studio**, our market-unique EDA toolset. If you use Studio, you may not only choose among the standard extensions defined by the RISC-V specification, but you can innovate by creating your own custom instructions and changing microarchitectural features. Studio enables you to verify your modified core and automatically generates a complete HDK and SDK.

Codalisp Studio flow





CODASIP BK3

The Balanced 32bit RISC-V Core

Codasip Bk3 has a single 3-stage pipeline architecture, providing a good balance between low power and performance, which reaches up to **3.1** CoreMark/Mhz. Supporting most RISC-V standard extensions for rich configurability, Bk3 presents an attractive alternative to legacy, proprietary microcontroller cores.

DELIVERABLES

SDK	<ul style="list-style-type: none"> • Compilation toolchain (LLVM) • C/C++ libraries • Simulators (instruction and cycle accurate)
HDK	<ul style="list-style-type: none"> • RTL • RTL simulation testbenches and run scripts • Synthesis scripts and constraints • Debugging tools (OpenOCD, LLDB)
Apps	<p>With source files, makefiles/Eclipse projects, and pre-compiled binaries:</p> <ul style="list-style-type: none"> • Set of example applications • Benchmarks (Coremark, Dhrystone)
Docs	<ul style="list-style-type: none"> • Datasheet • Manuals (Package, SDK...) • Specifications (ISA, Privilege, Debug...)

FEATURES

Base Integer ISA	RV32E/RV32I
Compressed ISA [C]	✓
Floating Point [F] (single precision)	Optional
Floating Point [D] (double precision)	N/A
Multiplication and Division [M]	Serial/Parallel
Atomic instructions [A]	N/A
Privilege modes	<ul style="list-style-type: none"> ✓ Machine ✓ User
Memory protection	Standard RISC-V PMP with up to 16 regions
Cache memory (instruction and data)	<ul style="list-style-type: none"> ✓ Custom cache size ✓ Custom line size ✓ Custom number of cache ways
Tightly coupled memory (instruction and data)	Each up to 2MB
Interrupt support	Up to 128 interrupt inputs
Branch prediction	N/A
JTAG & RISC-V debug support	4pin/2pin

OFF-THE-SHELF CONFIGURATIONS

The base 32bit integer instruction set (RV32I/E) can be obtained in the following pre-verified and immediately available configurations:

1. Base Integer Instruction Set (IMC)
2. Base Integer Instruction Set **with FPU** (IMFC)
3. **Embedded** Base Integer Instruction Set (EMC)

Bk3 architecture

