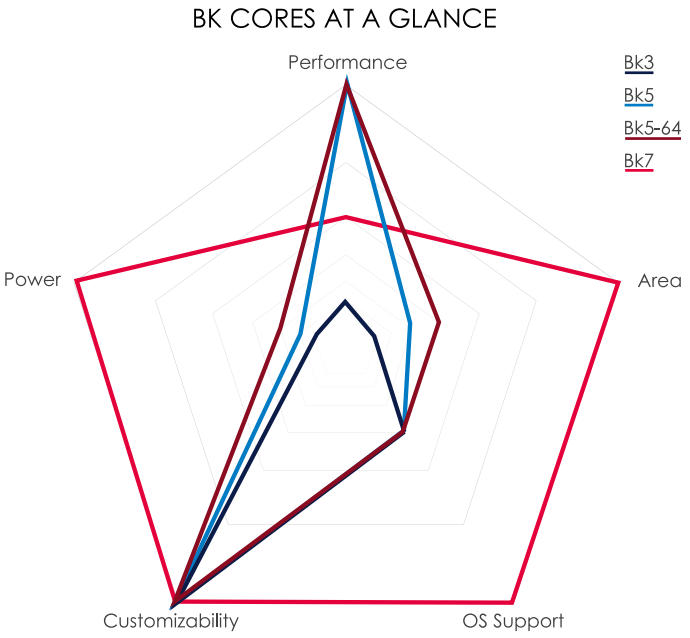
CODASIP
RISC-V Processors

If you are looking for an off-the-shelf RISC-V core, we offer a range of microarchitectural implementations of the RISC-V standard for virtually any application requirements. Codasip's own line of RISC-V processors, the **Bk family**, is fully verified and ready for instant deployment, or to be used as a quick-start base for customization with Studio.



RISC-V

The cornerstone of our processor family is the **RISC-V** ISA (instruction set architecture). It is an open, independent, royalty-free architecture that protects your investment in system software, thus minimizing risk.

Longevity

Established and supported by big industry players, RISC-V provides a strong, reliable, and growing ecosystem that is not dependent on a single vendor, which means that you will not have to face any incompatibilities and related redesign costs in the future. Traditional closed architectures now have a proven, credible alternative.

Innovation

Apart from being cost-efficient, RISC-V is also flexible. It includes base instructions that are always present, and a variety of standard extensions that you can choose from based on your specific needs. On top of that, RISC-V allows you to create novel custom instructions to achieve your performance, power or area goals and make your design truly unique.

THE ECOSYSTEM

Outstanding Software Infrastructure

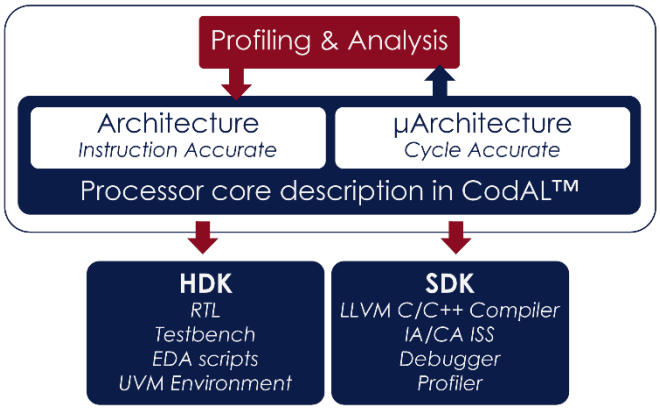
All Codasip cores are supplied with an industry-leading development environment, **Codasip CodeSpace**, for developing software to run on the designed processor. The IDE is based on the open Eclipse framework and it outperforms community alternatives across a wide range of benchmarks as we have added proprietary optimizations to its LLVM back-end.

Codasip CodeSpace includes a code editor, compiler, profiler, and debugger. You will get a 1-year license for free with any of our off-the-shelf RISC-V cores.

Customization with Studio

All Codasip Bk processors are fully verified and ready for instant deployment, or to be used as a quick-start base for customization with **Codasip Studio**, our market-unique EDA toolset. If you use Studio, you may not only choose among the standard extensions defined by the RISC-V specification, but you can innovate by creating your own custom instructions and changing microarchitectural features. Studio enables you to verify your modified core and automatically generates a complete HDK and SDK.

Codasip Studio flow



CODASIP **BK5**

The Versatile 32/64bit RISC-V Core

Codasip Bk5 has a 5-stage pipeline with optional caches and dynamic branch prediction, which allows it to run at higher frequencies without sacrificing performance—up to **3.2** CoreMark/MHz. Support for privilege-mode standard extension and memory protection unit or TCM makes it possible to run a variety of free and commercial RTOSs. The Bk5 variant with 64-bit address space and data support is ideal for modern data-intensive applications such as storage and networking.

DELIVERABLES

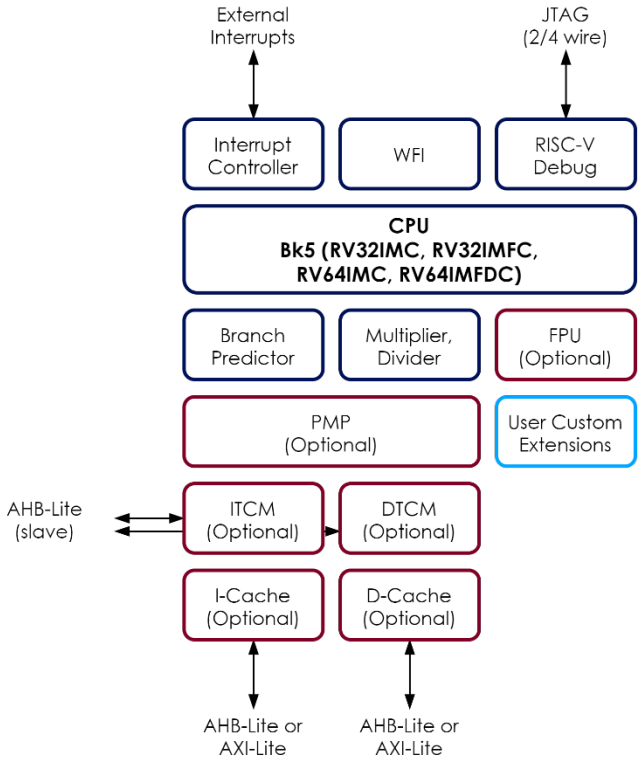
SDK	• Compilation toolchain (LLVM) • C/C++ libraries • Simulators (instruction and cycle accurate)
HDK	• RTL • RTL simulation testbenches and run scripts • Synthesis scripts and constraints • Debugging tools (OpenOCD, LLDB)
Apps	With source files, makefiles/Eclipse projects, and pre-compiled binaries: • Set of example applications • Benchmarks (Coremark, Dhrystone)
Docs	• Datasheet • Manuals (Package, SDK…) • Specifications (ISA, Privilege, Debug…)

OFF-THE-SHELF CONFIGURATIONS

The two variants of the base integer instruction set, 32bit and 64bit, can be obtained in the following pre-verified and immediately available configurations:

1. **32bit** Base Integer Instruction Set (32IMC)
2. **32bit** Base Integer Instruction Set **with FPU** (32IMFC)
3. **64bit** Base Integer Instruction Set (64IMC)
4. **64bit** Base Integer Instruction Set **with Double-Precision FPU** (64IMFDC)

Bk5 architecture



FEATURES

Base Integer ISA	**RV32I/RV64I**
Compressed ISA [C]	✓
Floating Point [F] (single precision)	Optional
Floating Point [D] (double precision)	Optional (with RV64I)
Multiplication and Division [M]	Parallel
Atomic instructions [A]	N/A
Privilege modes	✓ Machine ✓ User
Memory protection	Standard RISC-V PMP with up to 16 regions
Cache memory (instruction and data)	✓ Custom cache size ✓ Custom line size ✓ Custom number of cache ways
Tightly coupled memory (instruction and data)	Each up to 2MB
Interrupt support	Up to 256 interrupt inputs (with RV64I, 128 with RV32I)
Branch prediction	Dynamic
JTAG & RISC-V debug support	4pin/2pin