

# MYTHIC CASE STUDY

CUSTOMER	Mythic Inc., <a href="http://www.mythic-ai.com">www.mythic-ai.com</a>
DOMAIN	AI, DSP, co-processor control
PRODUCT	Codalisp L30™ processor, Codalisp Studio™
RESULT	Reusable programmable domain-specific core with custom instructions
PUBLISHED	February 2022

**Mythic**, the provider of a unique neural network accelerator based on analog computing, was designing an innovative Analog Matrix Processor (Mythic AMP™), the **M1076**, and found themselves in need of a small, power-efficient, yet programmable core to take care of specific supporting functions. As no off-the-shelf core exactly matched the needs and customization proved challenging, Mythic eventually opted for a complete solution from Codalisp: Using **Codalisp Studio**, an automated customization toolset, and the lightweight **Codalisp L30 processor core** as a starting point, Mythic got their optimized domain-specific core without compromises or delays.

*“Codalisp gave us the flexibility to create a truly unique RISC-V processor that was specific to our needs. This saved us the effort to build our own processor from scratch and allowed us to fully focus on other critical areas of the product development.”*

*Ty Garibay, VP of Hardware Engineering at Mythic*

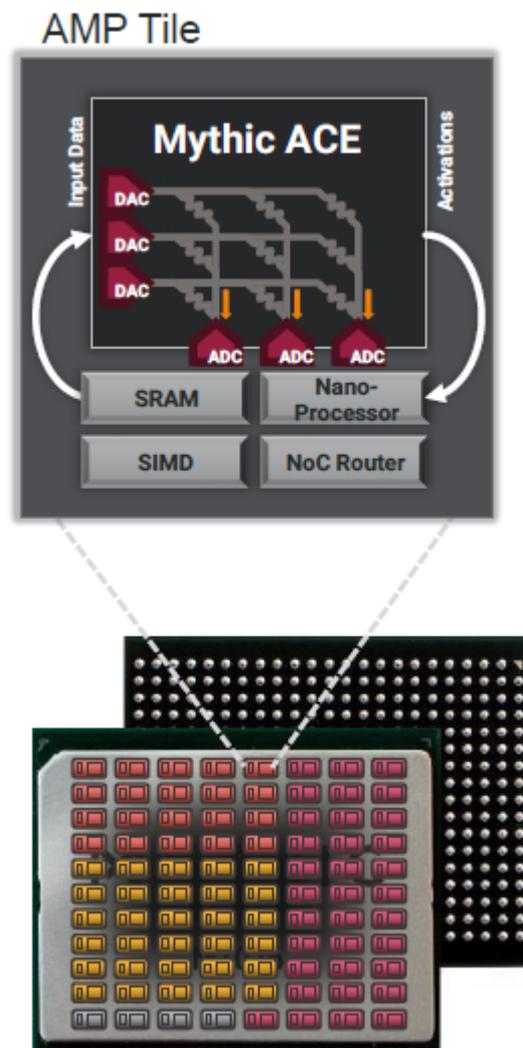


## 1 The Requirements

The Mythic Analog Matrix Processor (Mythic AMP™) M1076 integrates a large array of tiles. Each tile delivers unmatched performance, power, and flexibility. To achieve this, each tile combines:

- An Analog Compute Engine (Mythic ACE™).
- A processor, a SIMD engine, a scoreboard and local SRAM.
- A Network-on-Chip (NOC) router.

Each ACE stores neural network weights in non-volatile flash memory, which removes external memory storage requirements, and computes matrix multiplication directly inside the flash memory arrays, to avoid the waste of energy and time associated with significant movements of raw data.



*The Mythic Analog Matrix Processor (Mythic AMP™) M1076 integrates a large array of tiles. Source: Mythic.*

For the M1076 AMP, Mythic needed a small programmable core that would play a key role in the ACE. In each tile, the core would be required to:

- Manage and compute the data and resource dependencies required by the neural network model, with help from the hardware scoreboard.
- Manage and format the long-word workload commands based on the data sets and hardware resources.
- Sequence the workload commands to maximize throughput and minimize latency, when their trigger conditions are met.

A programmable core usually results in bigger area and higher power consumption, which Mythic wanted to avoid, as they needed to replicate the core over 80 times within the chip. To prevent expensive power and area demands that would result from the use of a less efficient core, Mythic started looking for a lighter one that would still offer the programmable capability.

## 2 The Challenge

Understandably, there was no off-the-shelf core that could provide exactly what Mythic needed. Creating one fully-in-house was a possible, but extremely time-consuming and risky option, so Mythic started looking for an outsourced solution. The main requirements were that:

- It was based on an **open architecture** to provide longevity and avoid high proprietary costs.
- It was **fully adaptable** to the specific needs of the product.
- It included all the necessary **tools** such as a **customized SDK** including **C compiler**.
- It included **verification** of the core, to avoid investing effort and own resources needed elsewhere.

## 3 The Solution

Codasip offered an optimal solution consisting of a configurable processor IP and a full configuration toolset with automated workflow. The Codasip processor IP is built on RISC-V, the proven open ISA with a rich supporting ecosystem. All Codasip off-the-shelf cores

are fully configurable and extensible. Mythic opted for **Codasip L30**, a small and efficient 32-bit core. L30 features a single 3-stage in-order execution processor pipeline and offers optional caches, IEEE 1149.1 debug, and industry standard bus interfaces.

To modify the core in line with their needs, Mythic also purchased a license for **Codasip Studio**, a complete, easy-to-use development toolkit for the processor customization. This market-unique tool automatically generates all related collateral, from RTL and testbenches through the functional verification environment up to a fully compatible SDK for the unique processor. Users can easily ensure compliance with the RISC-V standard. Using Codasip Studio for the L30 processor modification proved very helpful in terms of speed, ease, and reliability.

To start, Codasip provided a high-level description of a RISC-V micro-architecture implementation of the selected core.

Mythic's designers then described their desired architectural and ISA modifications in CodAL, Codasip's own architecture description language based on C.

The L30 processor core was configured with:

- RV32IC.
- Instruction cache only.
- Wide load/store interface.
- On-chip debugger.
- Low-latency interrupts.

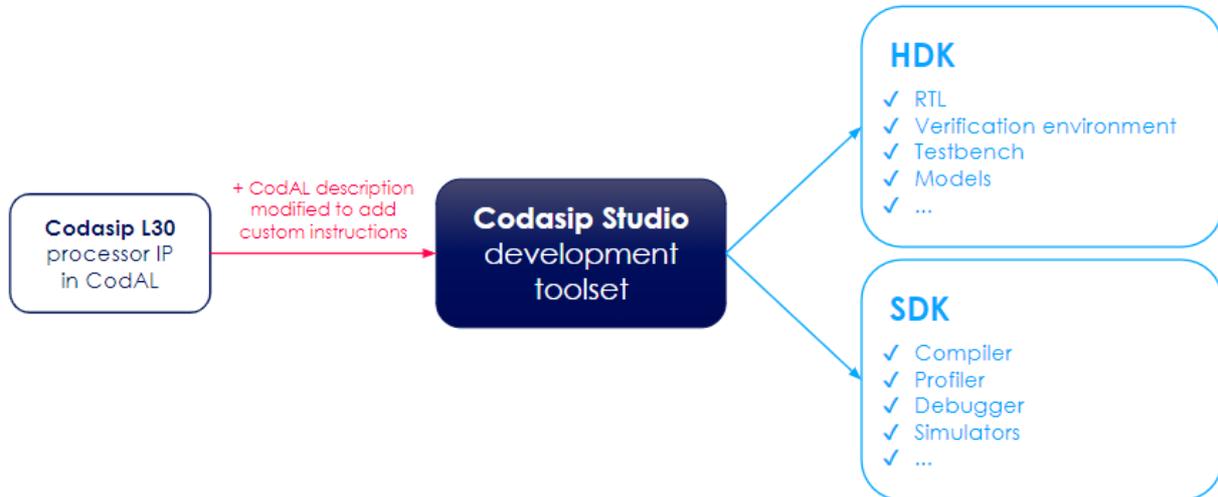
Mythic extended the core with the following types of instructions they required:

- DSP
- Bit manipulation
- Zero-overhead loops
- Coprocessor control instructions

Customization also included a coprocessor interface.

Once the CodAL description was final, Codasip Studio automatically synthesized the processor RTL, testbench, virtual platform models in SystemC, and processor SDK (C/C++ compiler, debugger, profiler, and other parts). Time that would otherwise be required to maintain a complete SDK and implementation was significantly reduced thanks to the methodology that uses an Instruction Accurate (IA) processor model in CodAL for SDK generation and a Cycle Accurate (CA) model for implementation.

From getting the specifications to finalizing the verified deliverables, it took less than two months.



*Codasip's customization solution. Source: Codasip.*

## 4 The Result

Codasip's unique customization methodology and tools enabled the creation of a domain-specific processor for the Mythic AMP™ M1076 with minimal cost and resource investment. Just as required, the core is cycle-efficient, low-power, low-area, and based on viable open-source technology. Mythic's goal was reached, and the M1076 can now add best-in-class intelligence to any device – without the need for access to the cloud, without high power consumption, and without expensive supporting chips in the system – by delivering powerful, local AI in a compact chip.

### About Mythic

Mythic aims to provide cutting-edge solutions that enable developers to build and deploy powerful, reliable AI for smart camera systems, intelligent appliances, brilliant robotics, and more. Mythic products are based on a unique, highly-parallel AI compute architecture that features three fundamental hardware technologies – Compute-in-Memory, Dataflow Processing, and Analog Computing. This innovative approach, along

with easy-to-use software tools, makes developing and deploying powerful AI easier and more affordable than ever before.

## About Codasip

Codasip delivers leading-edge RISC-V processor IP and high-level processor design tools, providing IC designers with all the advantages of the RISC-V open ISA, along with the unique ability to customize the processor IP. As a founding member of RISC-V International and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded and application processors. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has R&D centers in Europe and sales representatives worldwide. For more information about our products and services, visit [www.codasip.com](http://www.codasip.com).