Press Release

CODASIP BOOSTS STUDIO PROCESSOR DESIGN TOOLS WITH AXI AUTOMATION

Munich Germany, October 26, 2021 – Codasip, the leading supplier of customizable RISC-V processor IP, today announced further enhancements to its Studio processor design toolset. New features in Studio 9.1 include an expanded bus support with full AXI for high-performance designs, as well as improved support for LLVM and improved code density.

Studio is at the heart of Codasip's offering to simplify the task of customizing designs, enabling companies of all sizes to differentiate their products at the core. Studio has been the market leader in democratizing processor design since it was launched in 2014. Simplifying processor customization, Studio walks designers through the steps necessary to create their ideal custom RISC-V processor from a Codasip embedded or application core design – ensuring the design achieves predictable results and the highest performance.

Studio delivers these benefits to a rapidly expanding community of RISC-V developers around the world and, with today's launch of Studio 9.1, will extend this leadership enabling higher-performance and lower cost designs.

Specifically in 9.1, Studio users gain access to additional bus interfaces, to now include full AXI which means Studio will readily support the development of more powerful application cores and multi-core systems.

Instruction memory size can dominate cost in embedded processors so code density improvements in Studio 9.1 will help to contribute to reducing overall system costs.

Codasip's latest update incorporates the LLVM-based SDK (the fast C/C++ compiler, Linker Support Package – all of which were incorporated as part of Studio 9.0 launched in April 2021). This update significantly improves support for custom instructions in application cores running a rich OS, such as GNU/Linux. Another new feature brings support for ISA sub-targets that hugely reduce the maintenance of different SDKs for different ISA configurations.

Zdeněk Prikryl, Codasip CTO, said, "We are constantly evolving our tools offering and due to the nature of the diverse customer types, our projects and developments continue to help push our design tools further. Codasip is keen to simplify ***design for differentiation*** with our processor cores and tools which we have developed to make it easy for designers of any size to benefit from: enabling them to get high-performance, cost-effective and (importantly!) significantly differentiated products to market quickly and easily."

About Codasip

Codasip delivers leading-edge RISC-V processor IP and high-level processor design tools, providing IC designers with all the advantages of the RISC-V open ISA, along with the unique ability to customize the processor IP. As a founding member of RISC-V International and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded and application processors. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has R&D centers in Europe and sales representatives worldwide. For more information about our products and services, visit www.codasip.com. For more information about RISC-V, visit www.riscv.org.

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