Press Release

CODASIP ADOPTS IMPERAS FOR RISC-V PROCESSOR VERIFICATION

Outlines vision for best-in-class RISC-V quality

Oxford, United Kingdom & Munich, Germany – 22 November 2021 — Imperas Software Ltd., the leader in verification solutions for RISC-V, and Codasip, the leader in customizable RISC-V processor IP, today announced that Codasip has adopted Imperas reference designs and the Imperas DV solution for Codasip IP. Codasip has invested heavily into processor verification to deliver the industry's highest quality RISC-V processors.

Codasip has included Imperas golden reference models in its DV testbenches to ensure an efficient verification flow that accommodates a wide range of flexible features and options while scaling across the entire roadmap of future cores to enable rigorous confirmation of functional quality.

RISC-V is a modular architecture that offers many different permutations of base instructions, standard optional extensions and custom instructions - that raises concerns about implementations and the risk of fragmentation. Codasip's internal testing already uses an internal instruction-accurate model, several sources of direct and random testing (internal and externally provided), and several different technologies to check and ensure processor compliance. Imperas configurable reference models are already fully tested and enable all the configuration options needed to support this comprehensive view.

The Codasip engineering team based in Sophia-Antipolis, France, reviewed the challenges of the evolving RISC-V specifications, the full Codasip processor IP portfolio, extensions and configurable features, plus future roadmap plans. Imperas solutions were found to be ideal to support the operational workload and scale requirements. The Codasip engineering team set-up the infrastructure and test frameworks around

the Imperas RISC-V Reference Models to efficiently test all configurations with the ability to adapt for new roadmap features.

"Imperas are the pioneers in simulation technology and processor verification for RISC-V," said **Philippe Luc, Verification Director Codasip**. "While processor verification is not a new problem, there are many RISC-V suppliers, with customization and various levels of verification or conformance: customers are legitimately concerned about both quality and fragmentation. Codasip is very proud of our rigorous approach to verification– using Imperas as an important part of our quality process furthers extend our differentiation. The Imperas independence, reputation and technical strength provides our customers with further reassurance in our 'best in class' RISC-V processors,"

Simon Davidmann, CEO at Imperas Software Ltd, added, "Codasip provides the RISC-V market with a range of processor solutions that enable optimized performance for a wide range of applications. Design verification of this processor IP is fundamental to Codasip continuing to deliver the highest-quality processors as it moves to the next generation of its IP. Each additional optional feature roughly doubles the verification workload. The Imperas approach supports Codasip's development by applying Continuous Integration/Continuous Development to a sophisticated processor DV environment by using simulation and offers an efficiency advantage without compromising optional features. Imperas and Codasip share a common vision that improved quality is essential to the success of RISC-V."

Availability

The Imperas RISC-V Reference Models for Codasip are available now to lead customers and partners for software development and as a foundation for virtual platforms.

#RISCVSummit

The RISC-V Summit and DAC are co-located for 2021, December 6-8 in San Francisco, CA.

Codasip is a Platinum Sponsor for RISC-V Summit 2021, information about its attendance, our keynote and other presentations, and to arrange a meeting with our team, visit here

Imperas is a Diamond Sponsor for the RISC-V Summit 2021, more details on all the keynotes, talks and to request a demos are available at this link.

About Imperas

Imperas is the leading provider of RISC-V processor models, hardware design verification solutions, and virtual prototypes for software simulation. Imperas, along with Open Virtual Platforms (OVP), promotes open source model availability for a spectrum of processors, IP vendors, CPU architectures, system IP and reference platform models of processors and systems ranging from simple single core bare metal platforms to full heterogeneous multi-core systems booting SMP Linux. All models are available from Imperas at www.imperas.com and the Open Virtual Platforms (OVP) website.

For more information about Imperas, please see www.imperas.com. Follow Imperas on LinkedIn, twitter @ImperasSoftware and YouTube.

About Codasip

Codasip delivers leading-edge RISC-V processor IP and high-level processor design tools, providing IC designers with all the advantages of the RISC-V open ISA, along with the unique ability to customize the processor IP. As a founding member of RISC-V International and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded and application processors. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has R&D centers in Europe and sales representatives worldwide. For more information about our products and services, visit www.codasip.com. For more information about RISC-V, visit www.riscv.org.

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