codasip
STUDIO

Solving your on-chip processing challenges.

## DESIGN & CUSTOMIZATION TOOLSET

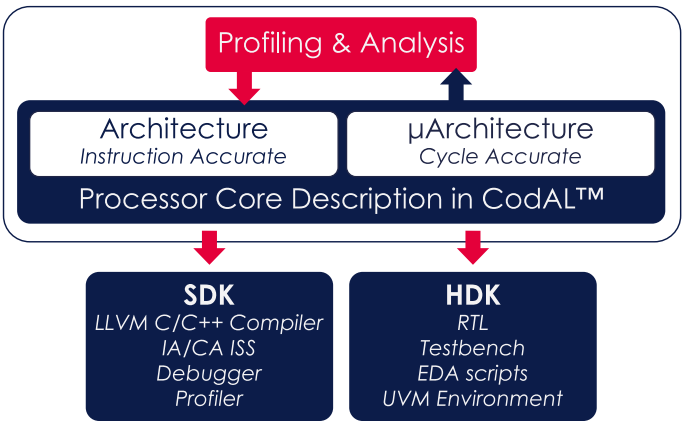
*Codasip Studio™ is a complete set of Electronic Design Automation (EDA) tools for processor design and customization. The level of automation is unmatched on the market and makes it possible to save considerable effort, time, and costs in all stages of processor development while achieving superior results.*

Codasip Studio employs a revolutionary approach to processor development: The design is captured in one single high-level description of the processor that replaces multiple manual tasks of writing the RTL, adding any custom instructions, updating the compiler, etc. Unlike similar tools, Codasip Studio generates the design implementation, verification environment, virtual system prototype, and a complete SDK fully automatically.

Codasip Studio is based on open standards and tools such as Eclipse, LLVM, Verilog, SystemVerilog, and UVM to ensure compatibility and longevity.

## PATENTED TECHNOLOGY

A unique aspect of our approach at Codasip is to automate the development of processor cores by using a *single description* of your processor capabilities, from which all deliverables are automatically generated. This description is written in **CodAL™**, a high-level processor description language similar to C. Everything needed to implement, verify, and program the processor is generated from the CodAL description, which eliminates the need to create the same functionality using manually written RTL, verification environments, and software toolchain. Together with its powerful multiprocessor programming, debugging, and profiling features, Codasip Studio makes it possible to design the most complex processors with ease.




*Codasip Studio flow*

## UNMATCHED EFFICIENCY

Traditionally, processor development is a complex and challenging process that takes weeks or months and ties up specialized and expensive resources. With Codasip Studio, many of the steps are highly automated which significantly reduces both design time and cost. Compared to traditional manual design of a custom ISA, Codasip Studio is an order of magnitude more effective, as shown in the customer example below.

| Deliverables | Codasip Studio | Manual design |
|---|---|---|
| Architectural exploration/ modelling | 40 –60 | 40 –60 |
| Toolchain/SDK creation | < 1 | 80 |
| Virtual platform | | 80 |
| Hardware implementation (RTL) | | 100 |
| UVM environment | | 30 |
| Verification | 40 –60 | 100 –150 |
| Total man-days | 80 –120 | 930–1010 |

*Processor development in man-days*

### Superior Results

Codasip Studio's powerful high-level processor synthesis technology allows you to generate processors that meet and even exceed the performance of hand-optimized designs. The ability to add domain-specific instructions natively into the processor pipeline delivers performance well above coprocessors, custom accelerators, and traditional extensible processor approaches.

Codasip Studio's simple-to-use, yet advanced profiling capabilities allow you to analyze your application code to determine potential optimizations to your design and to achieve the best possible PPA.

## CODASIP STUDIO BENEFITS

- ✓ Fully automated design flow
- ✓ Fully automated SDK generation
- ✓ Ability to optimize using in-built profiler
- ✓ Comprehensive processor description
- ✓ Quick start in a familiar C-based language
- ✓ Clean, human-readable RTL
- ✓ Automatically generated verification environment

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## COMPLETE TOOLCHAIN

Codasip Studio automatically generates a complete HDK and SDK customized for the processor. The SDK enables you to develop, debug, and execute firmware on the target platform well ahead of silicon availability.

### Hardware Development Kit (HDK)

- RTL (Verilog/VHDL/SystemVerilog)
- SystemVerilog UVM test environment
- Integration test bench
- Sample EDA scripts
- SystemC co-simulation model

### Software Development Kit (SDK)

- C/C++ LLVM compiler (enhanced by Codasip)
- C/C++ Libraries
- Assembler, disassembler, linker
- High-performance instruction set and cycle accurate simulators
- Debugger
- Profiler
- Documentation and ISA visualization
- Random programs used during verification

## RIGOROUS VERIFICATION

Strong verification methodology employed by Codasip Studio combines a standardized approach, simulation, and static checking for reliable results.

Codasip Studio provides a consistency checker, random assembler program generation and an automatically generated UVM environment. UVM allows the generated RTL for your processor to be checked against your instruction-accurate reference model.

Multiple model formats are available to ensure that at each step of the verification, you have the best trade-off between viability and performance. From virtual prototyping to detailed system debug, Codasip Studio generates the models you need.

## WAYS TO USE CODASIP STUDIO

Codasip Studio is both powerful and versatile. Getting started is easy when you select any of our ready-made Codasip RISC V Processors as a quick-start base for your own custom design. You can also start from scratch and create a fully custom processor of any type (RISC, CISC, VLIW, DSP…). You can optimize your existing core, too. Or you can use Codasip Studio just for painless maintenance of your legacy proprietary processor's SDK.

## CUSTOMER EXAMPLES

**Equalization algorithms for audio processing**

Design exploration in Codasip Studio suggested starting with RV32I instructions and extending the set with M and custom DSP instructions.

- ✓ Final result 56.24× throughput of original design
- ✓ Gatecount 2.43× greater than original design
- ✓ Codesize 3.62× smaller than in original design
- ✓ Significant saving in mask-making costs by targeting older coarser technology node

**Quantum-resistant security for low resource devices**

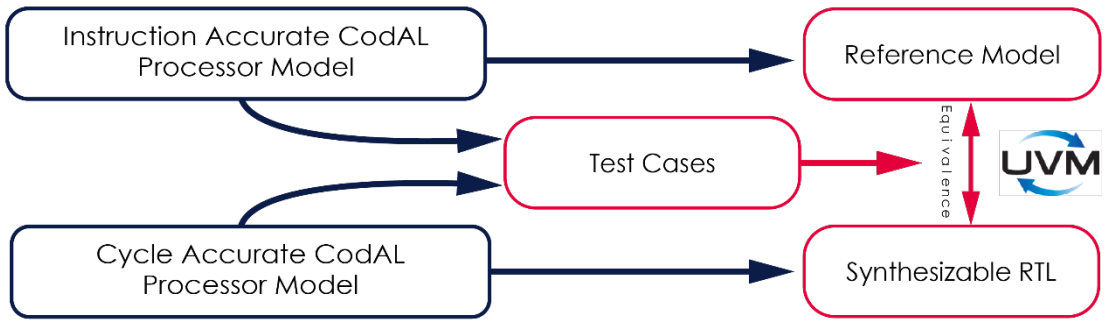
Accelerating a digital signature algorithm was achieved by adding *one instruction* to a Codasip RISC-V Processor:

- ✓ Final result 2.8× faster than the original design
- ✓ Gatecount 1.02× greater than original design
- ✓ Codesize 1.32× smaller than in original design

**Processor for a unique AI compute platform**

To achieve low power AI computation in a compact chip, Codasip Studio added custom extensions to a Codasip RISC-V processor (B, DSP, zero-overhead loops, and coprocessor interface instructions) to perform:

- ✓ General purpose tasks
- ✓ Domain specific tasks
- ✓ Offloading part of the DSP work




*Verification in Codasip Studio*