codasip
RISC-V PROCESSORS

Solving your on-chip processing challenges.

OUR PORTFOLIO & YOUR BENEFITS

All our processors are fully verified and ready for instant deployment, or to be used as a quick-start base for customization with Codasip Studio.

If you are looking for an off-the-shelf RISC-V core, we offer a range of microarchitectural implementations of the RISC-V standard for virtually any application requirements. For the embedded domain, we provide processors with focus on two different primary needs: small and efficient **Low Power Embedded** cores, and more powerful **High Performance Embedded** cores. In addition to these, we have the most advanced **Application** cores able to run Linux.

Each of the domains includes multiple series based on microarchitecture complexity.

Codasip RISC-V portfolio

THE POWER OF RISC-V

The cornerstone of our processor family is the **RISC-V** ISA (instruction set architecture). It is an *open, independent, royalty-free architecture* that protects your investment in system software, thus minimizing risk.

Longevity

Established and supported by big industry players, RISC-V provides a *strong, reliable, and growing ecosystem* that is not dependent on a single vendor, meaning that you will not have to face incompatibilities and related redesign costs in the future. Traditional closed architectures now have a proven, credible alternative.

Innovation

RISC-V is modular and flexible. It includes *base instructions* that are always present, and a variety of *standard extensions* that you can choose from based on your specific needs. On top of that, RISC-V allows you to create *custom instructions* to achieve your performance, power or area goals and make your design truly unique.

COMPLETE SOFTWARE ECOSYSTEM

Codasip cores are supplied with **Codasip CodeSpace™,** an industry-leading development platform for developing software to run on the designed processor. The IDE is based on the open Eclipse framework. It outperforms community alternatives across a wide range of benchmarks as we have added proprietary optimizations to its LLVM back-end.

Codasip CodeSpace includes a code editor, compiler, profiler, and debugger. You will get a *1-year license for free* with any of our off-the-shelf RISC-V cores.

Standard Buses

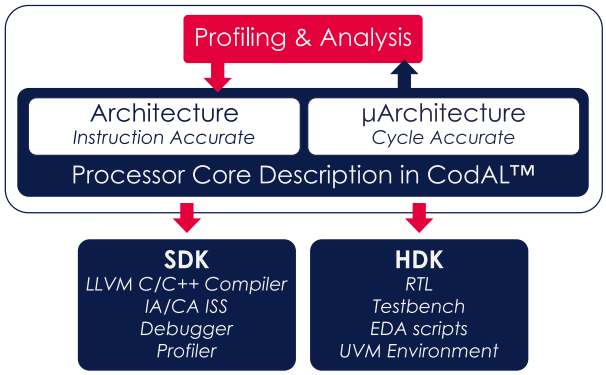
We provide native AMBA interface support for each processor. You can configure and customize the AHB-Lite or AXI-Lite interfaces, thus preserving your investments made in industry-standard peripheral IP blocks without taking the latency penalty that comes with using bus bridges.

EASY CUSTOMIZATION WITH CODASIP STUDIO

All Codasip processors can be either instantly deployed, or customized using Codasip Studio, our unique EDA toolset.

With Codasip Studio, you can easily add standard RISC-V extensions, or innovate by creating your own custom instructions and changing microarchitectural features. Codasip Studio is highly automated and makes the task fast and easy, so you can get own unique domain-specific processor with the optimal ratio of power, performance, and area.

Codasip Studio enables you to verify your modified core and automatically generates a complete customized HDK and SDK, achieving in days what would otherwise take weeks.



Codasip Studio flow

codasip

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THE SERIES

We offer the following pre-verified and immediately available configurations:

All cores ✓ Standard RISC-V debug ✓ JTAG (4pin/2pin) ✓ Compressed instructions ✓ AMBA buses	**Low Power Embedded** ✓ 32-bit ✓ Up to 128 interrupts	**High Performance Embedded** ✓ 64-bit ✓ 32-bit with performance-boosting features ✓ Up to 256 interrupts	**Application** ✓ 64-bit ✓ Floating point unit ✓ Linux support: • RV64GC ISA • Atomic instructions • Memory management unit • Supervisor privilege mode ✓ **Multicore options**
7 series ✓ 7–9-stage pipeline ✓ IMC instruction set ✓ 32 registers ✓ Branch predictor ✓ Parallel multiplier			Codasip **A70X**™ Codasip **A70XP**™ Codasip **A70X-MP**™ Codasip **A70XP-MP**™
5 series ✓ 5-stage pipeline ✓ IMC instruction set ✓ 32 registers ✓ Branch predictor ✓ Parallel multiplier	Codasip **L50**™ Codasip **L50F**™	Codasip **H50X**™ Codasip **H50XF**™	
3 series ✓ 3–4-stage pipeline ✓ IMC instruction set ✓ 32 registers ✓ Parallel multiplier	Codasip **L30**™ Codasip **L30F**™		
1 series ✓ 3-stage pipeline ✓ EMC instruction set ✓ 16 registers ✓ Sequential multiplier	Codasip **L10**™		
Notes	***X** = 64-bit, **F** = Floating Point Unit, **P** = RISC-V P Packed SIMD Extension, **MP** = Multiprocessing*		

Deliverables

SDK
- ✓ Compilation toolchain (LLVM)
- ✓ C/C++ libraries
- ✓ Simulators (instruction and cycle accurate)

HDK
- ✓ RTL
- ✓ RTL simulation testbenches and run scripts
- ✓ Synthesis scripts and constraints
- ✓ Debugging tools (OpenOCD, LLDB)
- ✓ Set of example applications
- ✓ Benchmarks (Coremark, Dhrystone)

Applications with source files, makefiles/Eclipse projects, and pre-compiled binaries:
- ✓ Set of example applications
- ✓ Benchmarks (Coremark, Dhrystone)

Docs
- ✓ Datasheet
- ✓ Manuals (Package, SDK…)
- ✓ Specifications (ISA, Privilege, Debug…)

Optional Memory Features

Memory protection	Standard RISC-V PMP with up to 16 regions
Cache memory (instruction and data)	✓ Custom cache size ✓ Custom line size ✓ Custom number of cache ways
Tightly coupled memory (instruction and data)	Customizable, each up to 2 MB