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SweRV CORE SUPPORT PACKAGE

Solving your on-chip processing challenges.

SWERV CORES MADE EASY

"Innovate and differentiate within your next semiconductor device. Turning to open IP has never been easier."

The SweRV Core™ Support Package from Codasip provides all of the components necessary to design, implement, test, and write software for a SweRV-based system-on-a-chip, including verification testbenches and IP, reference scripts for leading EDA flows, models for simulation and emulation, and software development tools—all backed by professional technical support.

GOING OPEN

The **RISC-V open ISA** (Instruction Set Architecture) is challenging the status quo by changing the way system-on-chips are designed. Employing RISC-V protects your investment in system software, thus minimizing risk. No longer is it necessary to depend on closed ecosystems or a single vendor.

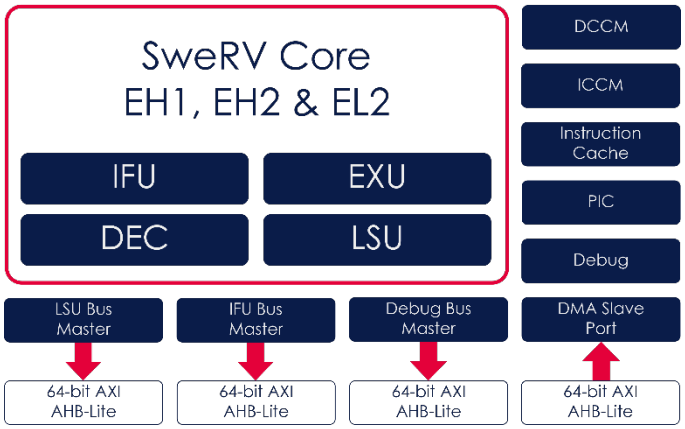
Open-source cores may be an attractive option for using RISC-V, as the RTL has no license fee. But it is important that you factor in the total cost of the core ownership. To use the open-source RTL, you will need to set up a comprehensive hardware implementation and verification flow. You will also need software development tools. We offer all this within our exclusive SweRV Core Support Package.

SweRV CORES

The SweRV Cores **developed by Western Digital** offer an impressive combination of performance and energy efficiency, and with the SweRV Support Package **provided exclusively by Codasip**, you can implement it into your chip at a fraction of the cost of competing technologies. We provide you with comprehensive support for commercial EDA design flows, covering everything you need to confidently deploy the core.

The SweRV Cores include medium to high-performance 32-bit RISC-V cores aimed at embedded applications such as storage controllers, industrial IoT, real-time analytics in surveillance systems, and other smart systems. The designs are power-efficient and capable of achieving high clock frequencies at the same time.

SweRV Core™



The Western Digital SweRV Core family currently consists of three members:

SweRV Core **EH1**

The Western Digital SweRV Core™ EH1 is a 32-bit, two-way superscalar, 9-stage pipeline core. With a performance of up to 5.7 CoreMark/MHz and small footprint, it offers you compelling capabilities for embedded devices that support data-intensive edge applications such as storage controllers, industrial IoT, real-time analytics in surveillance systems, and other smart systems. The power efficient design also offers clock speeds greater than 800 MHz on a 28nm CMOS process technology.

SweRV Core **EH2**

The SweRV Core EH2 was derived from the EH1. It adds dual threaded capability for additional performance, which reaches outstanding 7.8 CoreMark/MHz.

SweRV Core **EL2**

The SweRV Core EL2 is a small, ultra-low-power core with moderate performance, optimized for applications such as state-machine sequencers and waveform generators. With a performance of up to 4.3 CoreMark/MHz, it was designed to replace state machines and other logic functions in SoCs.

The SweRV Cores will be used in Western Digital products in the coming years. The design is open to utilize and contribute to.

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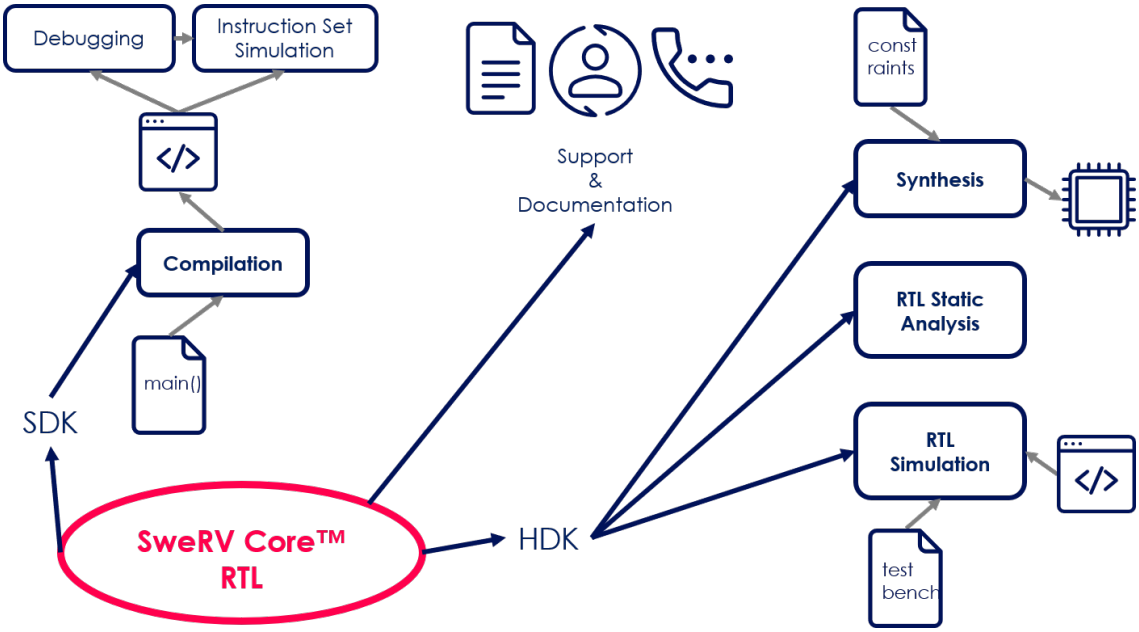
COMPLETE SUPPORT PACKAGE

The open sourcing of the SweRV Cores through CHIPS Alliance makes the cores very accessible to SoC designers. However open-source RTL alone is not sufficient to deploy a SweRV core in a design. A complete software toolchain as well as tested EDA flows are needed to utilize the core in an integrated circuit and to develop the corresponding firmware. Using a proven set of flows and toolchain is much more cost-effective than developing them from scratch.

The SweRV Support package contains everything needed to deploy a Western Digital SweRV Core in an integrated circuit, providing support for both EDA tool flows and embedded software development. The Support Package saves the considerable effort that would be needed to set up EDA flows for the SweRV cores from scratch. Predefined EDA flows are provided, with the differences between specific EDA tools abstracted from the user, and therefore easy to switch and update the flow as needed. The package is complete, supporting embedded software development, emulation, implementation, and comprehensive debug.

The SweRV Core Support Package is available in **Free** and **Pro** versions. The Free version consists of open-source deliverables and infrastructure for using open-source EDA tools and an SDK. The Pro version combines open-source and commercial deliverables. It provides flows, examples, and models for using popular commercial EDA tools. Codasip provides professional support for this version by e-mail and telephone. Verification of a modified RTL is offered as on-request service.



FREE VERSION

The free version of the package is aimed at educational and research use and features:

- ✓ Western Digital SweRV Core open RTL
- ✓ SoC example open RTL
- ✓ IP-specific flows for open EDA tools
- ✓ Western Digital Whisper ISS
- ✓ RISC-V GNU toolchain
- ✓ Eclipse IDE
- ✓ Open OCD debugging tool
- ✓ Software examples for SoC example
- ✓ Codasip infrastructure for EDA & IP

PRO VERSION

The pro version of the package is aimed at commercial SoC design and additionally features:

- ✓ Flows for commercial simulators
- ✓ Flows for commercial synthesis tools
- ✓ Flows for commercial RTL static code analysis
- ✓ Flows for equivalence checking
- ✓ Professional support from Codasip

Extra add-ons for SweRV Core EH1:

1. Floating-point unit (FPU), support for [F] and [D]
2. Data cache of configurable size (AXI / AHB-Lite)
3. Additional instructions for bit manipulation [B]