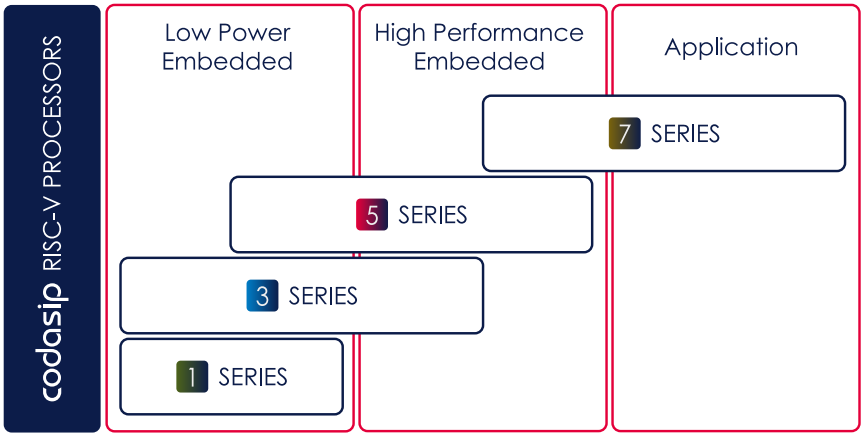
CODASIP RISC-V PROCESSORS
OUR PORTFOLIO & YOUR BENEFITS

All our processors are fully verified and ready for rapid deployment, or to be used as a quick-start base for customization with Codasip Studio.

If you are looking for an off-the-shelf RISC-V core, we offer a range of microarchitectural implementations of the RISC-V standard for virtually any application requirements. For the embedded domain, we provide processors with focus on two different primary needs: small and efficient **Low Power Embedded** cores (32-bit), and more powerful **High Performance Embedded** cores (64-bit). In addition to these, we have **Application** cores able to run Linux.

Each of the domains includes multiple series based on microarchitecture complexity.



Codasip RISC-V Processors portfolio.

THE POWER OF RISC-V

The cornerstone of our processor family is the **RISC-V** ISA (instruction set architecture). It is an *open, independent, royalty-free architecture* that protects your investment in system software, thus minimizing risk.

Longevity

Established and supported by big industry players, RISC-V provides a *strong, reliable, and growing ecosystem* that is not dependent on a single vendor, meaning that you will not have to face incompatibilities and related redesign costs in the future. Traditional closed architectures now have a proven, credible alternative.

Innovation

RISC-V is modular and flexible. It includes *base instructions* that are always present, and a variety of *standard extensions* that you can choose from based on your specific needs. On top of that, RISC-V allows you to create *custom instructions* to achieve your performance, power or area goals and make your design truly unique.

COMPLETE SOFTWARE ECOSYSTEM

Codasip cores are supplied with the **Codasip CodeSpace™** IDE and an SDK for the RISC-V core used. Codasip CodeSpace is a competitive platform for developing software and is based on the open Eclipse framework. The SDK includes an assembler/disassembler, compiler, linker, profiler, and debugger. The compiler outperforms community alternatives across a range of benchmarks due to proprietary optimizations to the LLVM back-end.

By using the RISC-V open ISA, users have access to a wide choice of embedded software, application software, and operating systems.

Standard Buses

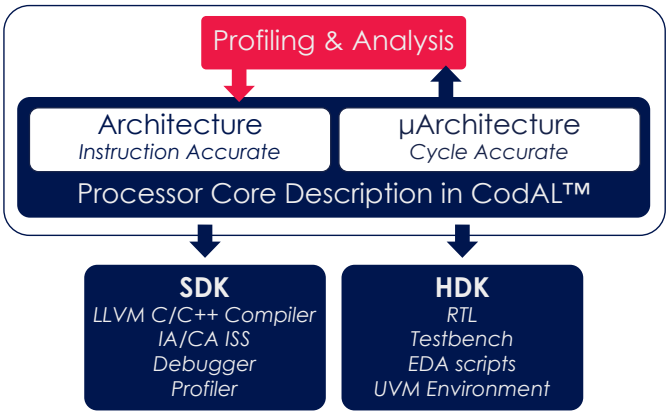
We provide native interface support of multiple AMBA protocols. You can configure and customize the interfaces, thus preserving your investments made in industry-standard peripheral IP blocks without taking the latency penalty that comes with using bus bridges.

EASY CUSTOMIZATION WITH CODASIP STUDIO

All Codasip processors can be either deployed rapidly, or customized using Codasip Studio, our unique EDA toolset.

With Codasip Studio, you can easily add standard RISC-V extensions, or innovate by creating your own custom instructions and changing microarchitectural features. Codasip Studio is highly automated and makes the task fast and easy, so you can get own unique domain-specific processor with the optimal ratio of power, performance, and area.

Codasip Studio enables you to verify your modified core and automatically generates a complete customized HDK and SDK, achieving in days what would otherwise take weeks.



Codasip Studio Flow.

DESIGN PROCESSORS SIMPLER, FASTER, AND CHEAPER.

THE SERIES

We offer the following pre-verified and immediately available configurations:

	ALL CORES Standard RISC-V debug JTAG (4pin/2pin) Compressed instructions AMBA buses	LOW POWER EMBEDDED 32-bit Up to 128 interrupts	HIGH PERFORMANCE EMBEDDED 64-bit Up to 256 interrupts	APPLICATION 64-bit FPU Linux support
7 SERIES	7-stage pipeline IMC instruction set 32 registers Branch predictor Parallel multiplier			Codasip A70 Codasip A70-MP Codasip A70P Codasip A70P-MP
5 SERIES	5-stage pipeline IMC instruction set 32 registers Branch predictor Parallel multiplier	Codasip L50 Codasip L50F	Codasip H50 Codasip H50F	
3 SERIES	3-stage pipeline IMC instruction set 32 registers Parallel multiplier	Codasip L31 Codasip L31F Codasip L30* Codasip L30F*		
1 SERIES	3-stage pipeline EMC instruction set 16 registers Sequential multiplier	Codasip L11 Codasip L10*		

** Not recommended for new designs*
F = Floating Point Unit, P = RISC-V P Packed SIMD Extension, MP = Multiprocessing

Deliverables

SDK
- ✓ Compilation toolchain (LLVM)
- ✓ C/C++ libraries
- ✓ Simulators (instruction and cycle accurate)

HDK
- ✓ RTL
- ✓ RTL simulation testbenches and run scripts
- ✓ Synthesis scripts and constraints
- ✓ Debugging tools (OpenOCD, LLDB)
- ✓ Benchmarks (Coremark, Dhrystone)

FPGA Evaluation Platform including peripherals

Applications with source files, makefiles/Eclipse projects, and pre-compiled binaries:
- ✓ Set of example applications
- ✓ Benchmarks (Coremark, Dhrystone)

Docs
- ✓ Datasheet
- ✓ Manuals (Package, SDK…)
- ✓ Specifications (ISA, Privilege, Debug…)

Optional Features

Memory protection: Standard RISC-V PMP with up to 16 regions

Cache memory (instruction and data)
- ✓ Custom cache size
- ✓ Custom line size
- ✓ Custom number of cache ways

Tightly coupled memory (instruction and data): Customizable, each up to 2 MB

Peripherals
Standard protocols (AMBA)
Expanding portfolio