A70

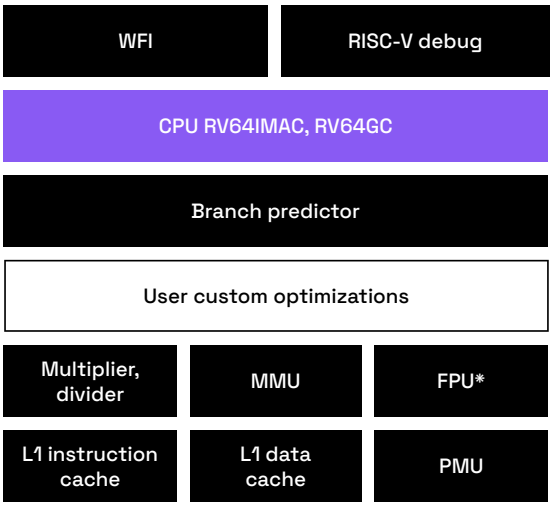
Product brief

Codasip

Overview

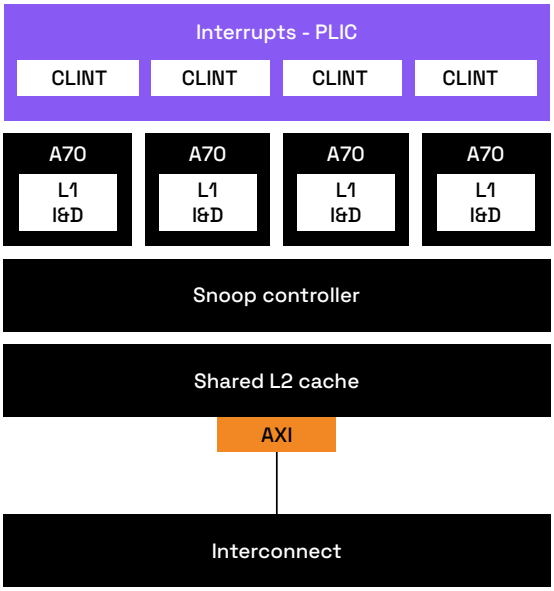
Codasip® A70 is a 64-bit RISC-V application processor. It includes a Memory Management Unit for supporting rich operation systems such as Linux. This power-efficient application core, also available in multi-core implementation, is targeting applications requiring high performance in power-constrained environments.

Codasip A70



*optional

Codasip A70 multi-core



Benefits

Linux capable

- For complex compute tasks, such as hosting a rich OS and supporting multiple software applications

Scalable and flexible

- Multiprocessing for higher performance while maintaining efficiency and flexible configuration options for diverse applications

Applications

Networking
Wearables
IoT nodes and gateways

→

Specifications

Core

- 7-stage, in-order pipeline
- RV64IMAC & RV64GC ISA
- 1 to 4 homogeneous cores in a cluster

Branch predictor

- Increased single-thread performance

Interrupts

- WFI
- NMI

L1 caches

- Instruction and data, optional
- Configurable cache size (any)
- Associativity (with any power of 2 cache ways) and line size (any power of 2, with minimum 16 bytes)
- Multi-core: Configurable cache size (16, 32, 64KB), 4-way associative, 32 or 64 bytes of line size

Memory protection

- Physical memory attributes with 2/4/8/16 regions
- MMU with up to 56 PA bits, 8 separate I&D TLB entries, fully associative, Sv39 translation scheme
- Customizable memory map
- Machine, Supervisor and User privilege modes

Debug

- Standard RISC-V debug 2/4 JTAG pins
- 2-8 breakpoints &
- watchpoints
- System bus access

L2 caches

- Multi-core only
- Shared cache
- Configurable cache size: 128KB-8MB in powers of 2
- Configurable associativity: 4/8/16 ways

Multiplier/divider

- Multiplier implementation: 2-cycle pipelined
- Divider implementation: Non- restoring

Interfaces

- Single-core: AHB3-Lite or AXI4-Lite with caches
- Multi-core: AXI4, 64 bits

Performance

- Performance monitors

Power

- Single-core: Block-level gating
- Multi-core: Clock gating in L2 cache