A730

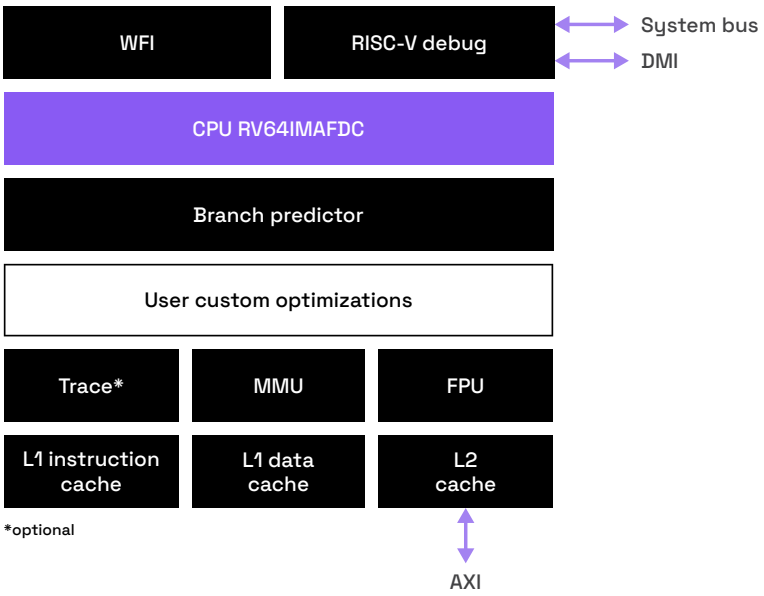
Product brief

Codasip

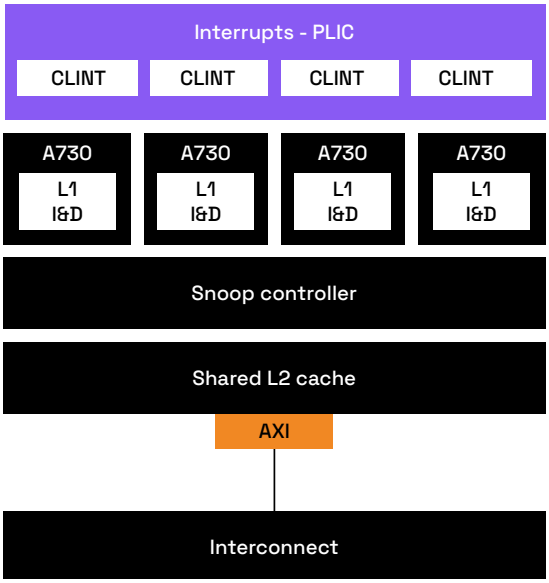
Overview

Codasip® A730 is a 64-bit RISC-V application processor. It includes a Memory Management Unit for supporting rich operating systems such as Linux. This mid-range processor is available in single-core and multi-core configurations with up to four cores in a cluster. Flexible, it targets applications that require performing complex compute tasks in power-constrained devices.

Codasip A730



Codasip A730 multi-core



Benefits

Flexible design

- Start your design with a competitive off-the-shelf core
- Flexibly configurable with Codasip Studio for advanced optimization
- Single or multi-core configurations

Ideal performance starting point

- Linux capable core
- 2x the performance of previous generation
- Dual-issue
- Faster, tightly-coupled cache coherent memory system

Broad market application

- Versatile core capable of Custom Compute
- Floating-Point Unit
- From edge IoT to AI and sensor fusion

→ Specifications

Core

- In-order, 7-stage, dual-issue pipeline
- RV64IMAFDC ISA
- RVA22 Compliant
- 1 to 4 homogeneous cores in a cluster
- Zcb for code-size improvement

Branch predictor

- Increased single-thread performance
- Configurable with area performance options

Interrupts

- WFI and NMI
- PLIC

L1 caches

- Private to the core
- Instruction and data
- 16, 32, or 64KB
- 4 ways

Memory protection

- Physical memory attributes with 8, 16, 32 regions
- MMU supporting Sv39 memory virtualization
- 16, 32, 64 instruction micro-TLB entries
- 16, 32, 64 data micro-TLB entries

Debug

- Standard RISC-V debug
- 4 debug triggers
- Debug Memory Interface (DMI) as an APB interface that can be used to interface with external debuggers
- System bus access

L2 cache

- Shared in multicore configurations
- 512KB to 2MB
- 4,8,16 associativity

Trace

- RISC-V standard E-trace interface
- Instruction and data trace
- Optional

Interface

- AXI-5 with atomic support
- 128 bits

Performance

- Performance monitors

Power

- Low-power design
- Always-on power domain
- Granular architectural clock gating