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L31AS

Product brief

Codasip

→
Benefits

Flexible use cases

- a Safety Island, as a protected enclave of the device providing freedom of interface for the independent execution of safety-related application code.
- a Controller, running the safety-related application code.

Based on Codasip L31

- silicon-proven embedded processor

Dual-core lockstep

- provides a robust and well trusted approach to building high-reliability systems and meeting the stringent safety requirements of critical applications

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Overview

Codasip L31AS is a 32-bit RISC-V embedded processor with TÜV SÜD ISO 26262 ASIL B certification. Part of our safety and security offering, this embedded processor is ideal either as a Main Controller or a Safety Island in a Functional Safety System. It includes 2 instances of Codasip L31 in a dual-core lockstep configuration along with Physical Memory Protection as a security feature.

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L31AS
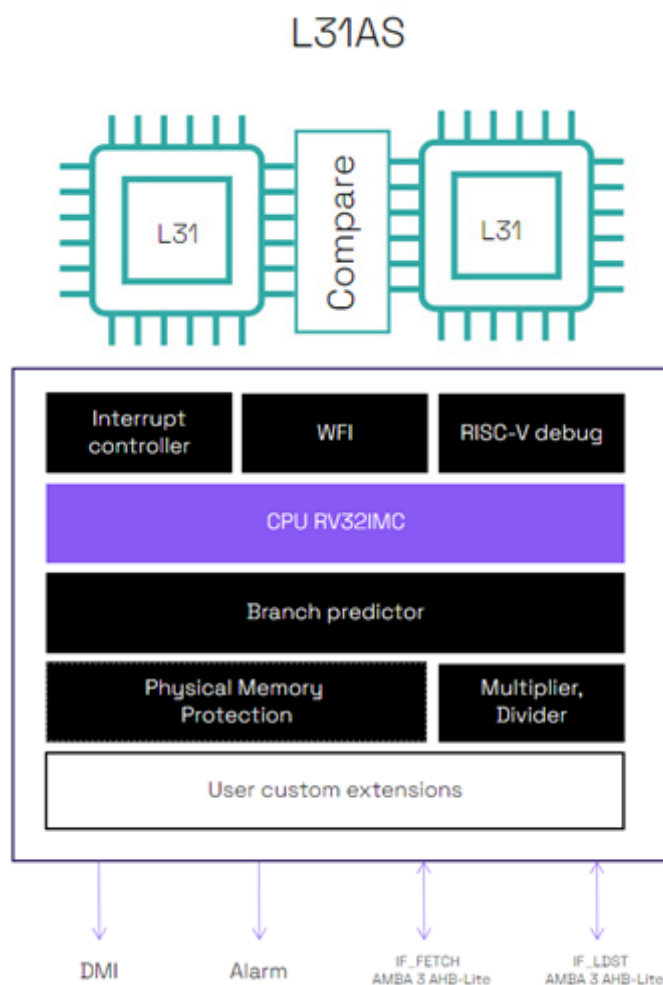
→ Specifications

Core

- In-order, 3-stage, single-issue pipeline
- RV32IMC ISA

Memory protection

- Physical memory attributes with 16 regions

Interrupts

- WFI and NMI
- PIC

Interfaces

- Separate Data and Instruction AHB-Lite Interfaces

Power & Performance

- Block-level gating in single-core configuration.
- Performance Counters

Debug

- Standard RISC-V debug
- 4 debug triggers
- Debug Memory Interface (DMI) as an APB interface that can be used to interface with external debuggers.
- System bus access

Safety Mechanism

- State of Art, Dual Core Lock Step (DCLS), with clock offset setting

Safety Pack

- Safety Manual
- Safety Case Report

Certification

- TÜV Süd ISO 26262 ASIL B