L110

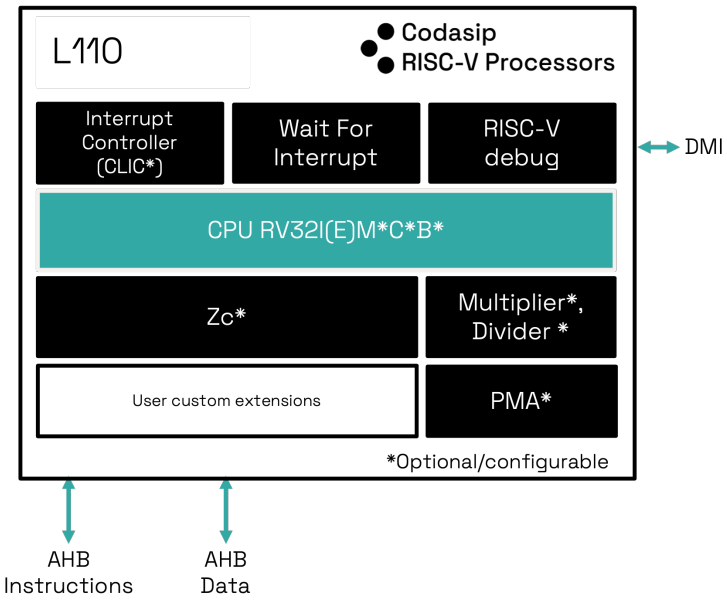
Product brief

Overview

Codasip® L110 is a 32-bit RISC-V embedded processor, focused on small-area and low-power applications.

The core is highly configurable, allowing different area and performance levels, with optional support for standard RISC-V code size density extension.

It is also fully customizable, and, when used in combination with Codasip Studio, it enables an easy and no-risk way to add custom instructions.



Benefits

- Ideal standard RISC-V IP for low area and low power applications, competitive in delivering performance per watt.
- Highly configurable with optional support for standard code size density extensions.
- Excellent base to add custom instructions to further improve power, performance, and area for specific target application.

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Specifications

Core

- In-order, 3-stage, single-issue pipeline
- Optional RV32I and RV32E baseline ISA

Memory protection

- Physical memory attributes with 16 regions

Interrupts

- WFI and NMI
- Configurable CLIC

Interface

- Separate Data and Instruction AHB-Lite Interfaces

Power & Performance

- Block-level gating in single-core configuration.
- Performance Counters

Debug

- Standard RISC-V debug
- 4 debug triggers
- Debug Memory Interface (DMI) as an APB interface that can be used to interface with external debuggers

Configuration Options

- RV32I/RV32E
- B Extension
- Multiplier (sequential and parallel)
- C Extension
- Zc Extension
- CLIC

Bounded Customization Support

- L110 can be used as tape-out quality baseline, in combination with Codasip Studio, to add Bounded Customization

HW Development Process

- Developed in compliance with ISO 26262 (ASIL D) and ISO/SAE 21434 standards