L150

Product brief

Overview

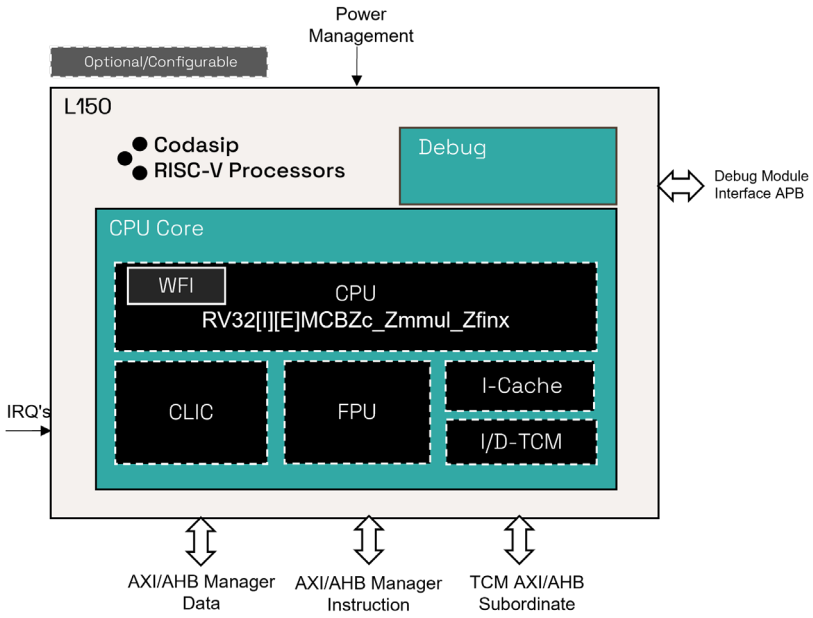
Codasip® L150 is a 32-bit RISC-V embedded processor, focused on real time small-area and low-power applications.

The core is highly configurable, allowing different performance points in the real time embedded space, including local memories for low-latency access, and including a tiny Floating-Point Unit (FPU) implementing Zfinx extension, as part of the RISC-V standard solution optimized for small cores.

The L150's is an excellent baseline to further accelerate domain specific applications, using Codasip's Bounded Customization technology, where custom instructions can be added with no risk to the functionality of the baseline core.

Benefits

- RISC-V RV32I compliant core achieving a very competitive performance/power balance for real time embedded applications.
- Highly configurable, with optional Tightly Coupled Memories, Caches and Zfinx extension.
- Excellent base for domain specific accelerations, such as DSP/AI application.



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Specifications

Architecture

- 32-bit, single-issue, 3-stage pipeline RISC V architecture
- Compliant with RISC-V RV32[E|I]MCB_Zc_Zmmul_Zfinx

Memory protection

- Physical memory attributes configurable with up to 16 regions

Interrupts

- Integrated Core Local Interrupt Controller (CLIC) configurable 4-512 interrupts with 0-255 priority levels
- Supports vector table for direct ISR addressing
- Supports preemption and nested interrupts

Interfaces

- Separate data and instruction: 32 bits AXI4-Lite/AHB3-Lite Memory Manager Interface
- 32 bits AXI4-Lite/AHB3-Lite core integrate subordinate interface for Tightly Coupled Memories (TCM)

Low power support

- Block-level clock-gating in single-core configuration
- Architectural defined sleep and power-down modes

Debug

- Standard RISC-V debug
- 2 or 4 debug triggers
- Debug Memory Interface (DMI) as an APB interface that can be used to interface with external debuggers (JTAG-APB bridge IP included)

Configuration options

- Configurable ISA
- Optional F (Zfinx) Extensions to increase computation capability
- Optional and configurable Tightly Coupled Data and Instruction Memories (TCM)
- Optional and configurable Instruction Caches

Bounded Customization support

- L150 can be used as tape-out quality baseline, in combination with Codasip Studio, to support custom instructions

HW development process

- Developed in compliance with ISO 26262 (ASIL D) and ISO/SAE 21434 standards