L735

Product brief

Codasip

Overview

The Codasip L735 is a 32-bit RISC-V embedded processor, built from the ground up with a focus on safety and security. It delivers benefits into all segments, especially automotive.

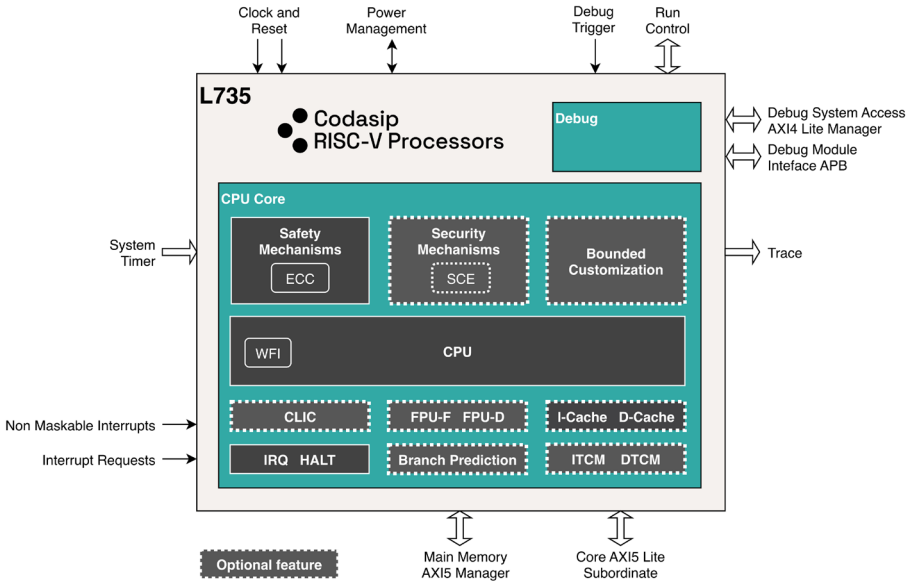
The core is highly configurable and has been certified up to ASIL B Automotive Safety Integrity Level by TÜV SÜD. It is ready for integration into systems where demonstration of highest levels of reliability and regulatory compliance are essential.

Codasip 700 Family processor's PPA can be further improved for specific applications using Codasip's Bounded Customization technology, enabling risk-free custom instruction extension.

Benefits

Reliability and compliance

- RISC-V RV32 compliant core achieves a very competitive performance/power balance in a wide range of real time embedded applications, including automotive.
- Highly configurable, with support for Safety Mechanisms such as Data redundancy (ECC) and parity on AXI interface enabling the achievement of ASIL B hardware metrics.
- Developed according to Codasip's IP development process which has been certified as compliant to both ISO 26262 and ISO/SAE 2134.



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Specifications

Architecture

- 32-bit, in-order, dual-issue, 9-stage pipeline RISC-V architecture
- Compliant with RISC-V RV32IMAFDCZcb

Memory protection

- Physical memory attributes configurable with up to 32 regions
- Optional Physical Memory Protection

Interrupts

- Integrated Core Local Interrupt Controller (CLIC). Configurable 16-512 interrupts with 0-255 priority levels
- Supports vector table for direct ISR addressing
- Supports preemption and nested Interrupts

Interfaces

- 64 bits AXI5-Lite Memory Manager Interface
- 64 bits AXI5-Lite Core Subordinate Interface for Tightly Coupled memories (TCM) and RAS Error Record Register Interface (RERI) access

Low power support

- Block-level clock-gating in single-core configuration
- Architectural Defined Sleep and Power-Down Modes

Debug

- Debug Memory Interface (DMI) as an APB interface that can be used to interface with external debuggers[1]
- Optional 32 bits AXI4-Lite Manager System Bus
- RISC-V E-trace Interface (Instruction Trace and Data Trace)

Nominal configuration options

- Optional F and D Extensions to increase computation capability
- Configurable Branch Predictor to tune single-thread performance: Branch Target Buffer (BTB), Branch History Table (BHT) and Return Address Stack (RAS)
- Optional and configurable Tightly Coupled Data and Instruction Memories (TCM)
- Optional and configurable L1 Data and Instruction Caches

Safety mechanisms

- ECC on Cache and TCM RAMs
- Parity on Branch Prediction RAMs
- Parity on AXI Interfaces

Optional security mechanisms

- Scalar Crypto Extension (SCE)

Bounded Customization support

- L735 can be used as tape-out quality baseline, in combination with Codasip Studio, to support Custom Bounded Instructions (CBI)

HW development process

- Developed in compliance with ISO 26262 and ISO/SAE 21434 standards

Certification

- TÜV Süd ISO 26262 ASIL B

[1] JTAG-APB bridge IP included