Press Release

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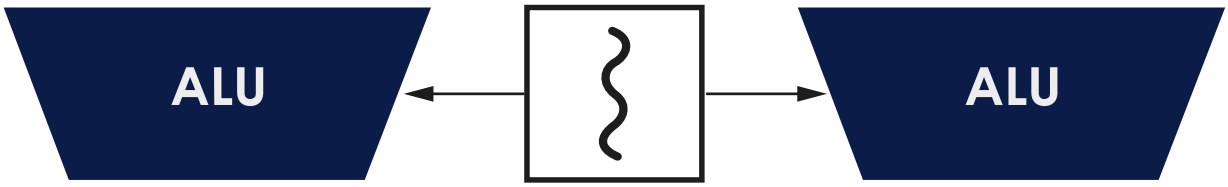
CODASIP® ANNOUNCES A71X RISC-V APPLICATION CORE WITH DUAL-ISSUE CAPABILITY

Munich, Germany – June 22, 2021 – Codasip, the leading supplier of customizable RISC-V® processor IP, today announces a new major version of its most advanced processor IP core: the A71X™ with dual-issue support for enhanced performance.

A71X is a RISC-V-based 64-bit core aimed at the application domain and able to run Linux. It is Codasip's first superscalar core, able to process instructions from one thread in two different execution units. This feature offers greatly improved performance, up to double the performance of a single-issue core.



Dual-issue core

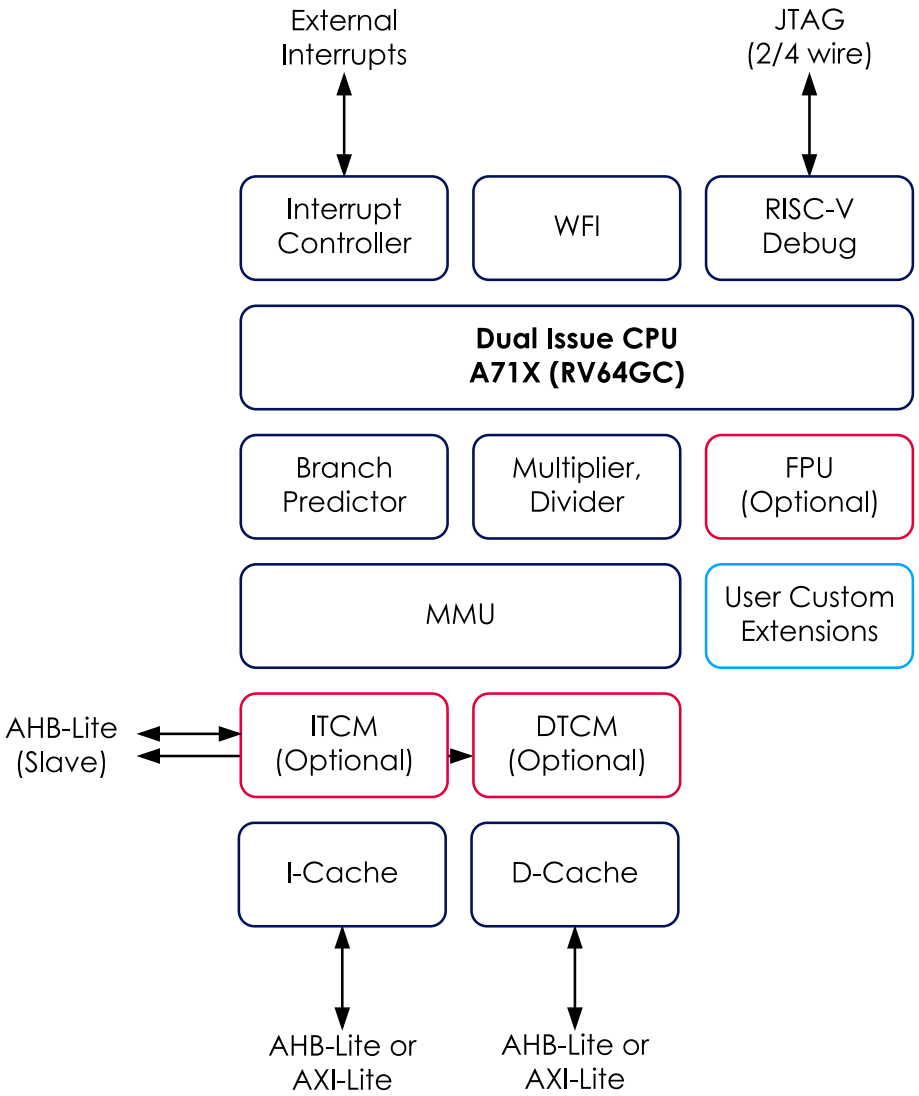
The configurations of A71X will include all microarchitectures that have already been announced for the earlier Codasip A70X™, including support for the RISC-V P extension and multi-core features. Together with the dual-issue capability, this will enable the design of powerful processors suitable for fast data-intensive applications in ML/AI, automotive, and similar domains.

"This is a very important addition to our application processor IP portfolio," says **Zdeněk Přikryl, CTO Codasip**. *"The new dual-issue capability will allow for a jump in performance without significant increase in power and area, which will make it possible to serve a much wider range of applications."*

All Codasip Application processor cores (those with code names beginning with "A") are 64-bit and use an AHB or AXI external interface. They also feature a Floating-Point Unit and Atomic instructions. All of them can run Linux as they support Machine, Supervisor & User privilege modes and have a Memory Management Unit.

All Codasip RISC-V cores for all domains (Low-Power Embedded, High-Power Embedded, and Application) are developed using Codasip Studio and provided as easy-to-customize CodAL models.

The A71X core and its configurations will be available towards the end of 2021.



Codasip A71X core

About Codasip

Codasip delivers leading-edge RISC-V processor IP and high-level processor design tools, providing IC designers with all the advantages of the RISC-V open ISA, along with the unique ability to customize the processor IP. As a founding member of RISC-V International and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded and application processors. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has R&D centers in Europe and sales representatives worldwide. For more information about our products and services, visit www.codasip.com. For more information about RISC-V, visit www.riscv.org.

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