Press Release

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CODASIP RELEASES A MAJOR UPGRADE OF ITS STUDIO PROCESSOR DESIGN TOOLSET WITH A TUTORIAL RISC-V CORE

Munich, Germany – April 13th, 2021 – Codasip, the leading supplier of processor design solutions and customizable RISC-V processor IP, is pleased to announce the availability of Codasip Studio 9.0 and Codasip CodeSpace 9.0. Key features include productivity improvements such as a new LLVM-based SDK with a fast C/C++ compiler, the Linker Support Package, and the tutorial 32-bit/64-bit uRISC-V processor.

Codasip Studio is a highly automated, market-unique toolset for processor design, optimization, and customization. Codasip CodeSpace is a complete platform for developing embedded software applications to run on a processor designed with Codasip Studio.

Codasip Studio 9.0 features an improved **LLVM-based SDK** including a fast C/C++ compiler, assembler, disassembler, and linker, with advanced support for debugging (DWARF format), and support for new ELF formats.

The **Linker Support Package** is a user-friendly interface for developing linker scripts, which represent a system memory map. Users do not need to understand the linker script language. This feature is available in both Codasip Studio 9.0 and Codasip CodeSpace 9.0.

A helpful new addition is the **tutorial uRISC-V Processor** that allows users to inspect and learn on a real RISC-V implementation. The architecture of the tutorial processor is RV32I[M] or RV64I[M] with 5 pipeline stages, and users can experiment with modifying the processor in Codasip Studio, adding custom instruction extensions and optimizing performance. The tutorial processor core was inspired by the book Computer Organization and Design RISC-V Edition: The Hardware Software Interface (ISBN 978-0128122754) by renowned authors David Patterson and John Hennessy. The tutorial is a part of Codasip Studio 9.0; for the earlier versions, it can be obtained as a separate package.

"Codasip Studio 9.0 is a major step forward in improving our processor development tool suite," said **Zdeněk Přikryl, Codasip CTO**. *"It comes with important new features that bring design productivity to the next level. The uRISC-V tutorial core can be a great vehicle for educational purposes or for familiarization with the RISC-V architecture in Studio."*

Other improvements include Eclipse-based development environment with a new look and feel, support for new operating systems and software (CentOS 8, Debian 10, Visual Studio 2019, new build system based on Python 3), and enhanced Physical Memory Attribute (PMA) support for caches.

About Codasip

Codasip delivers leading-edge RISC-V processor IP and high-level processor design tools, providing IC designers with all the advantages of the RISC-V open ISA, along with the unique ability to customize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded and application processors. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has R&D centers in Europe and sales representatives worldwide. For more information about our products and services, visit www.codasip.com. For more information about RISC-V, visit www.riscv.org.

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