

## CODASIP ANNOUNCES COMMERCIAL ADD-ONS TO SWERV CORE® EH1

**Munich, Germany – March 9<sup>th</sup>, 2021** – Codalip, the leading supplier of customizable RISC-V processor IP, announced three commercially licensed add-ons to the Western Digital SweRV Core® EH1. The add-ons enable the SweRV Core EH1 to be designed into a wider range of applications.

The SweRV Core EH1 is a 32-bit, dual-issue, RISC-V ISA core with a 9-stage pipeline, open-sourced through CHIPS Alliance. Codalip is now offering three add-on options to EH1:

- a) A floating-point unit (FPU) that supports the RISC-V single precision [F] and double precision [D] instructions.
- b) A data cache with configurable size, associativity, and cache lines. It can be configured with either AXI or AHB-Lite interfaces.
- c) Additional instructions for bit manipulation which can be beneficial for error detection/correction, DSP, and security algorithms.

*“The development of business models around open-source processor cores is following a similar path to the software world,”* explained **Karel Masařík, CEO of Codalip**. *“Commercially licensed add-ons to open-source software, such as IBM’s database software and middleware, are offered as paid options to Linux. We are providing three options to SweRV Core EH1 on a similar basis.”*

The SweRV Core EH1 is a powerful, two-way superscalar, 32-bit embedded processor core with a 9-stage pipeline. The SweRV Core EH1, along with the EH2 and EL2 cores, was developed by Western Digital. The deployment of these cores with commercial EDA tools and SDK is supported by Codalip’s [SweRV Core Support Package Pro](#). A free version is available through CHIPS Alliance on GitHub.

The SweRV Core EH1, EH2, and EL2 are available to the open-source community through [CHIPS Alliance](#), an open-source development organization which seeks to provide a barrier-free environment to allow collaboration for open-source software and hardware code. The EH1 has an optional 4-way set-associative instruction cache and optional instruction and data closely-coupled memories.

## About Cudasip

Cudasip delivers leading-edge RISC-V processor IP and high-level processor design tools, providing IC designers with all the advantages of the RISC-V open ISA, along with the unique ability to customize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and GNU-based processor solutions, Cudasip is committed to open standards for embedded and application processors. Formed in 2014 and headquartered in Munich, Germany, Cudasip currently has R&D centers in Europe and sales representatives worldwide. For more information about our products and services, visit [www.codasip.com](http://www.codasip.com). For more information about RISC-V, visit [www.riscv.org](http://www.riscv.org).

## About Western Digital

Western Digital creates environments for data to thrive. As a leader in data infrastructure, the company is driving the innovation needed to help customers capture, preserve, access, and transform an ever-increasing diversity of data. Everywhere data lives, from advanced data centers to mobile sensors to personal devices, our industry-leading solutions deliver the possibilities of data. Our data-centric solutions are comprised of the Western Digital®, G-Technology™, SanDisk®, and WD® brands.

## Media Contacts

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