Press Release

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VALTRIX AND CODASIP COOPERATE ON VERIFICATION OF RISC-V SYSTEMS

Bangalore, India and Munich, Germany – March 23rd, 2021 – Valtrix Systems, the provider of design verification products for building functionally correct CPU and system-on-chip implementations, and Codasip, the leading supplier of customizable RISC-V® embedded processor IP, announced today that they are cooperating on the verification of RISC-V-based systems.

The cooperation is based on applying the Valtrix STING product to add to Codasip's extensive methodologies for processor verification. STING's design verification capabilities are perfectly suited to verify processors, given its ability to generate portable self-checking stimulus across multiple device-under-test environments and to allow users to exercise architectural and micro-architectural features using its test stimulus programming framework.

"Complex CPU and SoC implementations require thorough verification before the products are released to the end user," said **Shubhodeep Roy Choudhury, Valtrix CEO**. *"STING provides a powerful and well-proven design verification methodology for testing the architectural compliance and functional correctness of RISC-V features and extensions. We are very proud to partner with Codasip and support their engineering teams with STING for their verification needs."*

"Codasip practices rigorous verification in order to ensure the quality of its processor IP products," said **Philippe Luc, Director of Verification at Codasip**. *"Codasip has always used multiple approaches in its verification strategy, and engaging with Valtrix and using the STING tools gives another complementary source of processor stimuli. Sting produces tests in a unique way on the market and can help uncover bugs before the release of our products."*

Codasip uses the combination of Codasip Studio, in-house tools, and third-party tools for processor verification. For example, processors are verified at the component level using dedicated random pattern generation and directed tests. At top level, architecture tests are used on top of in-house program generators. Consistency checkers ensure identical execution between the golden reference and the RTL. Formal techniques are also employed to ensure quality. Using the Valtrix STING product in this cooperation adds another level of testing to Codasip's RISC-V processors.

About Valtrix's STING Design Verification Tool

STING, the flagship product of Valtrix, is a design verification platform for RISC-V-based implementations. It can be configured to generate portable bare-metal programs containing self-checking architecturally correct test stimulus, which can then be enabled on simulation, FPGA prototypes, emulation, or silicon. STING also provides a RISC-V architecture verification suite to provide users an easy ramp into verification readiness. For more information on Valtrix's design verification technology and products, visit www.valtrix.in.

About Codasip

Codasip delivers leading-edge RISC-V processor IP and high-level processor design tools, providing IC designers with all the advantages of the RISC-V open ISA, along with the unique ability to customize the processor IP. As a founding member of the RISC-V Foundation and a long-term supplier of LLVM and GNU-based processor solutions, Codasip is committed to open standards for embedded and application processors. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has R&D centers in Europe and sales representatives worldwide. For more information about our products and services, visit www.codasip.com. For more information about RISC-V, visit www.riscv.org.

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