codasip	Western Digital SweRV		
	EH1	**EH2**	**EL2**
Architecture			
Pipeline stages	9	9	4
In-order/Out-of-order	in-order	in-order	in-order
Single/dual issue	dual	dual	single
Single/dual thread	single	dual	single
Number of registers	32	32	32
Instruction set			
Base instruction set	RV32I	RV32I	RV32I
Compressed instructions	Yes (standard RISC-V C extenstion)	Yes (standard RISC-V C extenstion)	Yes (standard RISC-V C extenstion)
FPU (single precission)	No	No	No
FPU (double precission)	No	No	No
Multiplication	Parallel (standard RISC-V M extenstion)	Parallel (standard RISC-V M extenstion)	Parallel (standard RISC-V M extenstion)
Division	Yes (standard RISC-V M extenstion)	Yes (standard RISC-V M extenstion)	Yes (standard RISC-V M extenstion)
Atomics	No	No	No
JTAG	4pin (standard RISC-V debug)	4pin (standard RISC-V debug)	4pin (standard RISC-V debug)
Branch predictor	Yes 2-8 level RAS 32/48/64/128/256/512 items in BTB	Yes 2-8 level RAS 32/64/128/256/512 items in BTB 32/64/128/256/512/1024/2048/4096 items in BHT	Yes 2-8 level RAS 32/64/128/256/512 items in BTB 32/64/128/256/512/1024/2048 items in BHT
Custom instructions	No	No	No
Memory			
Cache (instruction)	Optional Optional ECC 4 cache ways	Optional Optional ECC 2 or 4 cache ways	Optional Optional ECC 2 or 4 cache ways
Cache (instruction) size	16/32/64/128/256 kB	8/16/32/64/128/256 kB	8/16/32/64/128/256 kB
Cache (data)	No	No	No
Cache (data) size			
TCM (instruction)	Optional 8 banks	Optional 4/8/16 banks	Optional 2/4/8/16 banks
TCM (instruction) size	4/8/16/32/64/128/256/512 kB	4/8/16/32/64/128/256/512 kB	4/8/16/32/64/128/256/512 kB
TCM (data)	Optional 8 banks	Optional 2/4/8/16 banks	Optional 2/4 banks
TCM (data) size	4/8/16/32/48/64/128/256/512 kB	4/8/16/32/48/64/128/256/512 kB	4/8/16/32/48/64/128/256/512 kB
Memory protection			
MPU	No	No	No
Number of MPU regions			
Privilege mode	Machine	Machine	Machine
Interrupts			
PIC	Yes	Yes	Yes
NMI	Yes	Yes	Yes
Maximum number of external interrupts	255	255	255
Wake-up Interrupt Controller	limited, active waiting	limited, active waiting	limited, active waiting
Other			
Bus Protocol	AXI	AXI	AXI