CUSTOMER	Microsemi, now part of Microchip
DOMAIN	Audio processing
PRODUCT	Codasip L30™ processor, Codasip Studio™
RESULT	Reusable RISC-V low-power core with custom instructions
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Microsemi was developing an audio processing unit for the IoT. They were interested in replacing an off-the-shelf core and wanted to evaluate the flexibility of RISC-V in addressing their processing needs. Using **Codasip Studio**, our automated customization toolset, and the lightweight **Codasip L30 processor core** as a starting point, they profiled their echo cancellation software and then looked at different ISA scenarios.

1 The Requirements

Microsemi needed a low-cost, low-power processor core that would replace an existing Cortex-M processor core. The new core would be the baseline for creating derivative designs.

2 The Challenge

Microsemi were looking to create a new generation of IoT connected audio processing devices. The products needed to achieve the following:

- Achieve the necessary performance for echo-cancelling algorithms
- Consume low power
- Avoid high manufacturing costs such as using a small geometry process.
- Use mainstream design methods and process node.

Microsemi was interested in the free, open RISC-V ISA for multiple reasons. Firstly it avoided vendor lock-in and thereby ensured that investments in software would be protected for the future. Secondly, they saw the potential in RISC-V's modularity and custom instructions that could allow them to tailor a processor design to their algorithmic workload.

3 The Solution

Codasip offered an optimal solution consisting of a customizable processor IP and a full customization toolset with automated workflow. The Codasip processor IP is built on RISC-V, the proven open ISA with a rich supporting ecosystem. All Codasip off-the-shelf cores are fully customizable and extensible. Microsemi opted for **Codasip L30**, a small and efficient 32-bit core. L30 features a single 3-stage in-order execution processor pipeline and offers optional caches, IEEE 1149.1 debug, and industry standard bus interfaces.

To modify the core in line with their needs, Microsemi used **Codasip Studio**, a complete, easy-to-use development toolkit for the processor customization. This market-unique tool automatically generates all related collateral, from RTL and testbenches through the functional verification environment up to a fully compatible SDK for the unique processor. Users can easily ensure compliance with the RISC-V standard. Using Codasip Studio for the L30 processor modification proved very helpful in terms of speed, ease, and reliability.

	Clock Cycles	Code size	Area (Gates)	Speedup vs. RV32-IM	Area vs. RV32-IM	Speedup vs. RV32-IM	Area vs. RV32-IM	Speedup vs. RV32-IM-p	Area vs. RV32-IM-p
L30, RV32-I	1,764,256	232	16.0k	-	-	-	-	-	-
L30, RV32-IM (sequential multiplier)	427,561	148	19.7k	4.12x	1.24x	-	-	-	-
L30, RV32-IM-p (single clock-cycle multiplier)	133,061	148	26.2k	13.26x	1.64x	3.21x	1.32x	-	-
L30, RV32-IM-DSP-p	**31,371**	**64**	**38.7k**	**56.24x**	**2.43x**	**13.62x**	**1.96x**	**4.24x**	**1.48x**

Figure 1 Iterations of the design exploration

Microsemi explored the L30 design with Codasip Studio, starting with just the RV32I base integer instructions. Then, through an iterative approach, they extended the instruction set with M and then custom DSP instructions. In the table above (Figure 1), the initial row is the baseline, then each row is the next variant of the design. Figure 2 shows the tradeoff between cycle count and gatecount for the configurations and custom instructions that were tried.

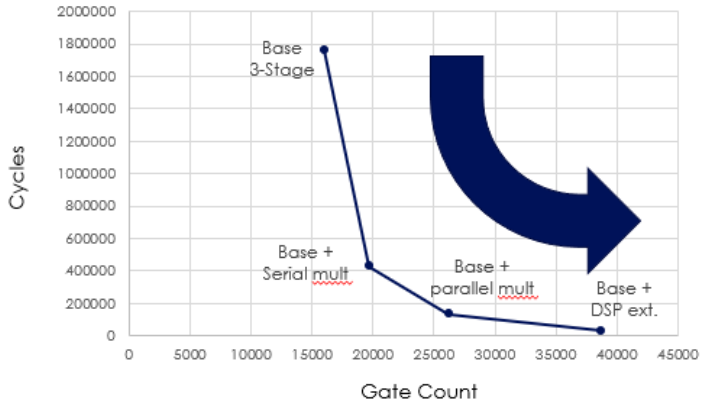

Figure 2 Benefits of custom instructions

Because the base 32-bit RISC-V ISA implementation is a minimal set of just 40 instructions, the core was small at 16 kgates. However, it was unlikely that RV32I would give the performance required and with almost 1.8M clock cycles for their test was too many.

The high clock frequency required would have resulted in too much power dissipation. Since their DSP algorithm included many multiplications, the next obvious step was to add the [M] multiplication/division optional extensions. The use of the RV32IM combined with a sequential multiplier improved performance but was well below the design's target. Using a parallel multiplier helped bring performance to over 13× faster than the RV32I design.

Finally, they experimented with custom DSP extensions. The custom instructions increased the throughput 56.24× over the original RV32I at the cost of making the core 2.43× bigger in gate count. The increased throughput meant that a slower clock frequency was needed thereby reducing dynamic power.

With embedded systems, the silicon area is dominated by instruction memory and hence code size matters. The use of custom instructions reduced the code size from 232 kbytes to 64 kbytes, an improvement of 3.62×.

4 The Result

Codasip's unique customization methodology and tools enabled the creation of a custom processor core for Microsemi with minimal cost and within the required power envelope. Just as required, the core is cycle-efficient, low-power, and based on viable open-source technology. Microsemi's goal was reached, without using a more advanced process node, and their custom core can add audio-processing capabilities to IoT devices.

About Codasip

Codasip delivers leading-edge RISC-V processor IP and high-level processor design tools, providing IC designers with all the advantages of the RISC-V open ISA, along with the unique ability to customize the processor IP. Codasip is committed to open standards for embedded and application processors. We were a founding member of RISC-V International and we are a long-term supporter of LLVM And GNU-based toolchains. Formed in 2014 and headquartered in Munich, Germany, Codasip currently has R&D centers in Europe and sales representatives worldwide. For more information about our products and services, visit www.codasip.com.