Codasip FPGA evaluation platforms

Easily evaluate any of the Codasip RISC-V processors using our FPGA evaluation platforms in just a few minutes.

Our FPGA evaluation platforms help you easily assess our RISC-V IP. We provide one platform for embedded cores and one platform for application cores. Both will get you started and have your first C program running in 15 minutes.

One platform consists of the selected processor IP with a subsystem containing peripherals and AMBA interconnect. The FPGA top layer includes a clock generator and DDR controller for external memories, and integrates some of the FPGA peripherals, such as microSD card. Each platform is distributed either as a bitstream targeting the supported FPGA boards or as source code.

A Codasip FPGA evaluation platform includes:

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<td>Bare-metal demos, Linux image and sources (application cores only), RTOS (embedded cores only), FSBL sources</td>
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<td>ROM initialization file with FSBL</td>
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Embedded core evaluation platform

This AHB-based platform is provided for evaluating our low-power and high performance embedded cores. You can use it for system evaluation with either bare-metal software or RTOS (such as FreeRTOS).

Application core evaluation platform

This AHB or AXI-based platform is provided for evaluating single or multi-core systems based on our application cores. The platform comes with an embedded Linux image and support documentation for Linux compilation and user applications.

Single-core systems target simple boards. Multi-core systems require more complex boards.

Get your evaluation package

To get more information and receive your evaluation package, please contact our team at contact@codasip.com.