

### Design and customization toolset

Codasip Studio is a unique collection of tools for fast and easy designing or modification of processors. Introduced in 2014, it is silicon-proven by major vendors. All-in-one, highly automated, Codasip Studio is perfect for you to efficiently and cost-effectively customize an existing Codasip® RISC-V processor or design your own processor from scratch.

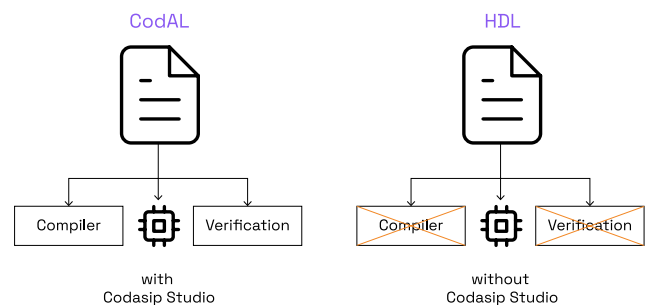
### Benefits

- Comprehensive processor description
- Description in familiar C-based language
- Fully automated SDK generation
- Analyze software using in-built profiler
- Clean, human-readable RTL generated
- Automatically generated verification environment
- Fully automated design flow

Codasip Studio is based on open standards and tools such as Eclipse, LLVM, Verilog, SystemVerilog, and UVM to ensure compatibility and longevity.

### Our technology foundation

With Codasip Studio, automate processor design and development by using a single description of the processor capabilities. The description is written in CodAL™, a high-level processor description language similar to C. Everything needed to implement, verify, and write software for the processor is generated from the CodAL description automatically.



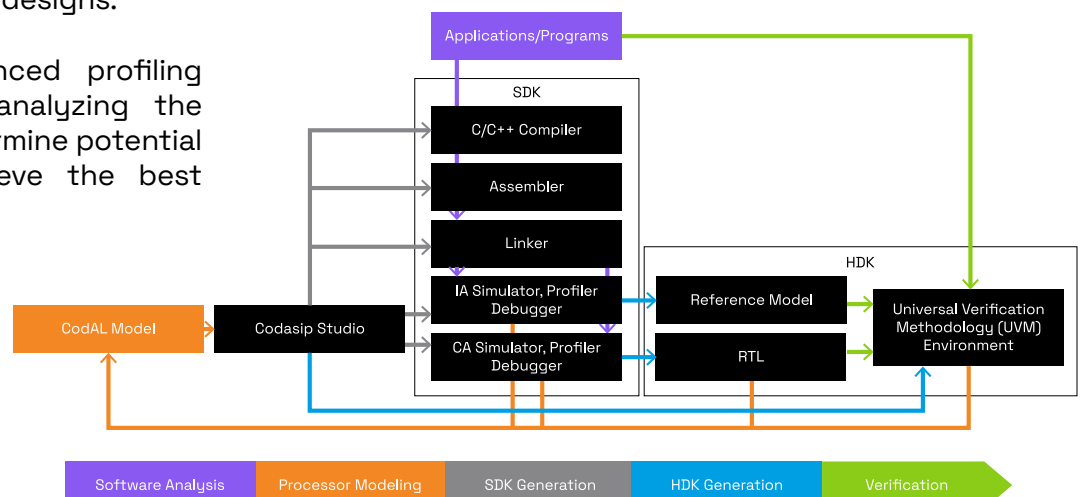
### A complete toolchain

Codasip Studio automatically generates a complete HDK and SDK customized for the processor. The SDK enables you to develop, debug, and execute firmware on the target platform well ahead of silicon availability.

### Better, unique PPA

Codasip Studio adds domain-specific instructions natively into the processor pipeline and features powerful high-level processor synthesis technology. The performance of generated processors exceeds hand-optimized designs.

Codasip Studio's advanced profiling capabilities allow for analyzing the application code to determine potential optimizations and achieve the best possible PPA.

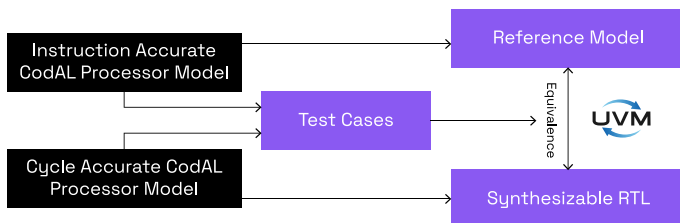


## Rigorous verification

Strong verification methodology employed by Codasip Studio combines a standardized approach, simulation, and static checking for reliable results.

Codasip Studio provides a consistency checker, random assembler program generation, and an automatically generated UVM environment.

UVM allows the generated RTL for your processor to be checked against your instruction-accurate reference model. Multiple model formats are available to ensure that at each step of the verification, you have the best trade-off between viability and performance. From virtual prototyping to detailed system debug, Codasip Studio generates the models you need.



## Ways to use Codasip Studio

Codasip Studio is both powerful and versatile, enabling you to use it in a way that best suits your needs:

1. Getting started is easy when you select any of our **ready-made Codasip RISC-V Processors** as a quick- start base for your own custom design.
2. You can also start from scratch and create a fully custom processor of any type (RISC, CISC, VLIW, DSP and others).
3. You can optimize your **existing core** described in CodAL, too.
4. Or you can use Codasip Studio just for painless **maintenance** of your legacy proprietary processor's SDK.



## Customer examples

### Equalization algorithms for audio processing

Design exploration in Codasip Studio suggested starting with RV32I instructions and extending the set with M and custom DSP instructions:

- Final result 56.24× throughput of original design
- Gatecount 2.43× greater than original design
- Codesize 3.62× smaller than in original design
- Significant saving in mask-making costs by targeting older coarser technology node

### Quantum-resistant security for low resource devices

Accelerating a digital signature algorithm was achieved by adding one instruction to a Codasip RISC-V Processor:

1. Final result 2.8× faster than the original design
2. Gatecount 1.02× greater than original design
3. Codesize 1.32× smaller than in original design

### Processor for a unique AI compute platform

To achieve low power AI computation in a compact chip, Codasip Studio added custom extensions to a Codasip RISC-V processor (B, DSP, zero-overhead loops, and coprocessor interface instructions) to perform:

- General purpose tasks
- Domain specific tasks
- Offloading part of the DSP work

## Happy customers include

**Rambus**

**MYTHIC**

**in** mobileye  
An Intel Company

**Microsemi**

**DONGWOON**  
ANATECH